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SUPERCONDUCTING MATERIAL FOR IR DETECTOR ARRAYS

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Northrop Grumman – along with a major subcontractor at the University of Cincinnati – performed a 4-year program for the Air Force Research Laboratory (AFRL) to develop and evaluate high-T superconducting (HTS) materials for infrared detector arrays. The use of HTS materials and devices in infrared (IR) detectors was motivated by the very long wavelength cutoff at the superconducting energy gap (greater than 40 micron), immunity of superconductors to many radiation environments, and very fast response times. In addition, they offered the potential for Josephson-based preprocessors with analog-to-digital converters (ADC) operating at three orders of magnitude lower power than comparable semiconductors ADCs. Such low-power ADCs are an enabling technology for on-focal-plane (FPA) digitization of IR images and low-noise transfer of digital signals to off-plane images.

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SUPERCONDUCTING MATERIAL FOR IR DETECTOR ARRAYS

Executive Summary

Objective

Northrop Grumman – along with a major subcontractor at the University of Cincinnati – performed a four-year program for the Air Force Research Laboratory to develop and evaluate high-T_c superconducting (HTS) materials for infrared detector arrays. The use of HTS materials and devices in IR detectors was motivated by the very long-wavelength cutoff at the superconducting energy gap (~ 40 μm), immunity of superconductors to many radiation environments, and very fast response times. In addition, they offered the potential for Josephson-based preprocessors with analog-to-digital converters (ADC) operating at three orders of magnitude lower power than comparable semiconductor ADCs. Such low-power ADCs are an enabling technology for on-focal-plane (FPA) digitization of IR images and low-noise transfer of digital signals to off-plane image processors .

TRW and the NASA Jet Propulsion Laboratory have demonstrated an on-focal-plane ADC circuit technology with niobium nitride-based superconducting ADCs operating at 10K. This low operating temperature limits potential applications to a few special types of detectors. In contrast, HTS devices can operate at temperatures up to 77K, making them compatible with a variety of detector types.

The specific objectives of the program were to:

- Determine the yield and reproducibility requirements for HTS Josephson junctions to be used in:
  – two-dimensional arrays as individual detector elements
  – on-FPA Josephson-based readout and digitization circuitry
- Develop HTS junctions with the required yield and reproducibility
- Fabricate 2-dimensional arrays of Josephson junctions in various configurations to permit an evaluation of their response to IR radiation
- Model the response of Josephson arrays to IR and compare with experiment
- Develop the integrated circuit technology needed to combine junctions in a low-power ADC circuit

- Demonstrate the type of circuit needed for on-FPA digitization

Accomplishments

The major accomplishments of this program are:

- Step-edge-grain-boundary (SEGB) and edge SNS (superconductor/normal-metal/superconductor) junctions were developed in parallel in the first year of the program. The SEGB junction effort was discontinued in favor of the SNS junctions since the spread of critical currents in sets of nominally identical junctions were smaller for the SNS configuration. At that point of the program, the standard deviation of critical currents for SEGB and SNS junctions were approximately 30% and 16%, respectively.
- Northrop Grumman demonstrated the first multilayer integrated circuit process for digital HTS circuits using the SEGB junction technology. This process required that the junctions were fabricated either on or above an HTS groundplane. Approximately a year later, Northrop Grumman and Conductus, Inc. became the first laboratories to develop the integrated groundplane process for SNS junctions and we agreed with Conductus to publish our separate papers in the same issue of *Applied Physics Letters.*
- SNS junctions with world-best reproducibility (based on spreads in critical current) were fabricated with YBCO and related rare-earth-BCO electrodes and with several doped-YBCO normal-layers. The range of materials for electrodes and N-layers allowed us to model the device physics and compare device performance with a standard proximity effect model for S-N interfaces.
- Two-dimensional junction arrays were fabricated and sent to the University of Cincinnati for evaluation. We fabricated arrays in both SEGB and SNS configurations and in a variety of n x m junction dimensions. Arrays were fabricated with both square and hexagonal lattices. Arrays were also fabricated with defects (missing junctions) deliberately inserted to allow direct comparison of experiment with models of defective arrays.
- During the last three years of program performance, Northrop Grumman participated in a consortium of the three leading institutions in development of HTS integrated circuit technology. Called the "Big Three" by several of the Government's technical representatives, the group was composed of Northrop Grumman, Conductus, and TRW. The group exchanged technical information prior to publication on a schedule with intervals never longer than 3 months. We developed standard test vehicle designs, automated test routines, visited each others laboratories at least once each year, exchanged samples, and compared processes. The result was a greatly accelerated rate of progress.

- This program produced the HTS digital circuit with the highest reported junction count. It was a 4-bit counting A/D converter with 39 HTS junctions. The counting ADC architecture consists of an input quantizer followed by a chain of toggle flip-flops – four, in this case – that can be read in parallel to produce a four-bit count proportional to the input signal strength. All 39 junctions, the quantizer, and all four toggle flip-flops functioned in our circuit.

Contents of This Report

Detailed descriptions of the accomplishments of the program are contained in the appendices of this report:

- Appendix A: Project-Supported Publications
- Appendix B: List of Project-Supported Presentations
- Appendix C: Project Personnel
- Appendix D: University of Cincinnati Report: Transport Properties of HTS Junction Arrays

Appendix A: Project-Supported Publications

The technical effort reported in most of these publications was supported wholly or in part by USAF Contract No. F33615-93-C-5355. Several of our other publications are included here in the cases of review articles or because the effort derived from the USAF program.

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HTS JOSEPHSON JUNCTION DEVELOPMENT

Josephson junctions are the fundamental building blocks for a variety of superconducting electronics applications, including high-speed, low-power digital logic, and sensitive magnetic field and high-frequency electromagnetic detectors. A Josephson junction consists of a "weak" connection between two superconductors which exhibits the Josephson effects (described below). While low-temperature superconductor (LTS) Josephson junction technology is well-developed, high-temperature superconductor (HTS) Josephson junctions are still relatively immature. Nonetheless, extensive HTS junction fabrication efforts are in progress due to the possibility of applying Josephson effects at temperatures compatible with reliable, low-cost refrigerators. In this article we discuss the more common approaches to HTS junction fabrication and optimization, with a focus on potential digital circuit applications.

Introduction to Josephson Junctions

According to the Bardeen–Cooper–Schreiffer (BCS) theory of superconductivity, the electrons in a superconductor are weakly bound into Cooper pairs and can be described mathematically by a complex wave function with spatially dependent amplitude and phase. The fact that all of these electrons occupy a macroscopic quantum state leads to several profound properties of superconductivity, such as zero resistance, quantization of the magnetic flux threading a hole in a superconductor, and the Josephson effects.

If two pieces of superconductor, each characterized by their own wave function, are brought very close together, but separated by a thin insulating layer, then the two wave functions can overlap. It was predicted by Brian Josephson (1) that this overlap would lead to novel phenomena associated with the dissipationless tunneling of Cooper pairs through the insulating barrier. The first of these, the direct current (dc) Josephson effect, is that a dc current can flow through this "Josephson junction" without the appearance of a voltage drop across the junction, and furthermore that the magnitude of this "supercurrent" is a function of the phase difference between the two electrodes. The maximum value of the supercurrent is called the critical current, I_c. Josephson's second prediction was that if a dc voltage were applied across the junction, then the phase difference would evolve at a rate proportional to the voltage, leading to a time-oscillating Cooper pair current. This is the alternating current (ac) Josephson effect.

Most of the above discussion can also be applied in cases where two superconducting electrodes are separated not by an insulator, but by other nonsuperconducting or weakly superconducting regions. These include normal metals, semiconductors, or even extremely narrow superconducting constrictions. This broader class of Josephson devices is generally known as "weak links," and essentially all HTS Josephson devices being developed fall under this heading. In particular, the use of a normal metal, or of a superconductor above its transition temperature, is the focus of much of the development work, and thus of the discussion in this article.

HTS versus LTS Materials

Fabrication of HTS Josephson junctions is complicated by the materials properties of the high-temperature superconductors. Low-temperature superconductor junctions are typically produced using polycrystalline metallic Nb as the superconductor. In contrast, the new HTS materials are multicomponent ceramic oxides with four or more elements, such as yttrium–barium–copper–oxide ($YBa_2Cu_3O_{7-x}$ or YBCO). The oxide superconductors have perovskite-based crystal structures with two to three copper–oxygen planes in a layered structure within a unit cell. As a consequence, these materials are anisotropic, with higher critical current densities and longer superconducting coherence lengths parallel to the CuO_2 planes. The superconductive coherence length is the characteristic length over which the Cooper pair density decays, as for example in approaching an interface between a

superconductor and a normal metal. It also corresponds to the average physical separation of the two electrons which make up a Cooper pair. For a clean material (mean free path much longer than coherence length) it is given by the approximate expression $\xi \approx 0.18\hbar v_F/k_B T_c$, where v_F is the Fermi velocity and T_c is the superconducting transition temperature (1). In contrast to most LTS materials, the coherence lengths in the oxide superconductors are on the scale of atomic dimensions (≈30 Å parallel to the copper oxide planes, and ≈4 Å perpendicular to the planes). Since damaged layers thicker than the coherence length result in degraded superconducting properties, surface cleaning and film growth at device interfaces are especially critical in the HTS materials.

Also unlike in most low temperature superconductors, grain boundaries in the HTS oxide superconductors lead to reduced critical current densities, and in fact can behave like Josephson junctions (see the section entitled "HTS Josephson Junction Types"). Because of the anisotropy and grain boundary problems associated with the high-temperature superconductors, epitaxial (single crystal) HTS films grown at high temperatures (650°C to 800°C) are required for many applications. High-temperature growth and the need to maintain high epitaxial quality in each layer of multilayer structures make HTS junction and circuit fabrication considerably more complex than the corresponding LTS processes.

Selection of YBCO for HTS Junctions

Nearly all Josephson junction development in HTS materials has been based on YBCO or nearly identical compounds with another rare-earth element in place of yttrium. The superconducting critical temperature, T_c, for this family of compounds is approximately 90 K. The main advantage of using YBCO compared with other HTS material families is the low volatility of all cation elements which permits films to be grown in a single step from a source—for example, a laser ablation target or sputtering target—fabricated with a stoichiometric ratio of yttrium, barium, and copper.

In contrast, films of the HTS families with the highest critical temperatures, Tl–Ba–Ca–Cu–O (TBCCO) and Hg–Ba–Ca–Cu–O (HgBCCO), are typically prepared in a two-step process in which a Tl- or Hg-deficient as-deposited film is annealed to the point of partial melting in a container sealed to obtain a high pressure of Tl or Hg vapor. Although grain boundary junctions can be formed by using this technique with bicrystal substrates or substrates with patterned steps, it is not extendible to multilayers. In the case of the Bi–Sr–Ca–Cu–O (BSCCO) or Ba–K–Bi–O (BKBO) families, films can be produced in a single step, but the volatility of K and Bi has limited film reproducibility and has discouraged junction development efforts. The TBCCO, HgBCCO, and BSCCO materials are also more highly anisotropic than YBCO, which introduces additional complications in 3-D structures.

Basic HTS Josephson Junction Characterization

The current–voltage characteristic for an ideal Josephson junction described by the Resistively-Shunted-Junction (RSJ) model is shown in Fig. 1. The RSJ model adequately describes the behavior of many HTS junctions, as explained in more detail in the section entitled "Josephson Effects." The primary junction parameters of interest are the critical current, I_c, the normal state resistance, R_n, and the product of these two factors, I_cR_n. The critical current is the maximum current that can flow through the junction without a voltage drop, while the normal state resistance is given by the inverse of the slope of the I–V characteristics at a few times I_c, as shown in Fig. 1. R_n is due to dissipation in the device, for example, by current flow through the normal metal in a superconductor/normal metal/superconductor weak link. I_c and R_n are often expressed in terms of area-normalized quantities: the critical current density, $J_c = I_c/A$, and the resistance–area product, R_nA. Characterization for an HTS Josephson junction typically includes (a) measurement of the current–voltage (I–V) characteristics as a function of temperature and (b) measurement of I_c modulation in a magnetic field. In some cases, the I–V characteristics are also studied under microwave irradiation as a measure of the ac Josephson effect. In a well-behaved HTS junction the I–V shape will show the concave-up curvature consistent with the resistively shunted junction model. The temperature dependence of I_c and R_n gives information on the nature of coupling across the Josephson junction (e.g., proximity-effect coupling or tunneling), while the dependence of I_c on magnetic field provides a gauge of the uniformity of Cooper pair transport across the weak link. More comprehensive Josephson junction studies can also include determination of the J_c dependence on tunnel barrier or interlayer thickness, as well as measurement of J_c uniformity across multiple junctions on a chip (important for circuit applications).

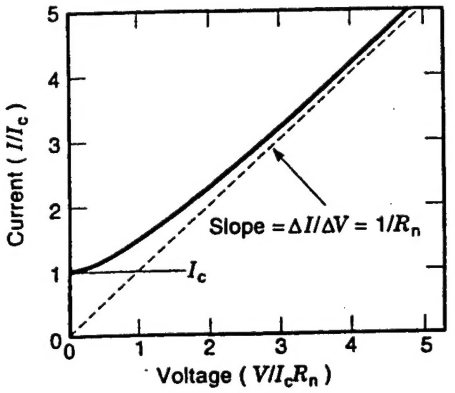

Figure 1. Current–voltage characteristic of a Josephson weak link in the zero-capacitance limit, without thermal noise, showing definitions of the critical current, I_c, and normal resistance, R_n. The dashed line is the high-current asymptote of the I–V curve.

Survey of Junction Configurations

Josephson effects in HTS materials were first observed at naturally occurring grain boundaries in films and in weak links between two HTS samples created by either breaking a sample in vacuum and coupling across the vacuum gap or bringing two pieces in contact and coupling through a surface layer that was degraded by reaction in air. Most of the configurations used since that time to fabricate junctions with controllable and reproducible properties are shown in Fig. 2. All configurations require epitaxial films to prevent naturally occurring and randomly placed grain-boundary junctions from interfering with the engineered junctions. The fill pattern for HTS film layers in Fig. 2 indicates the orientation of Cu–O planes.

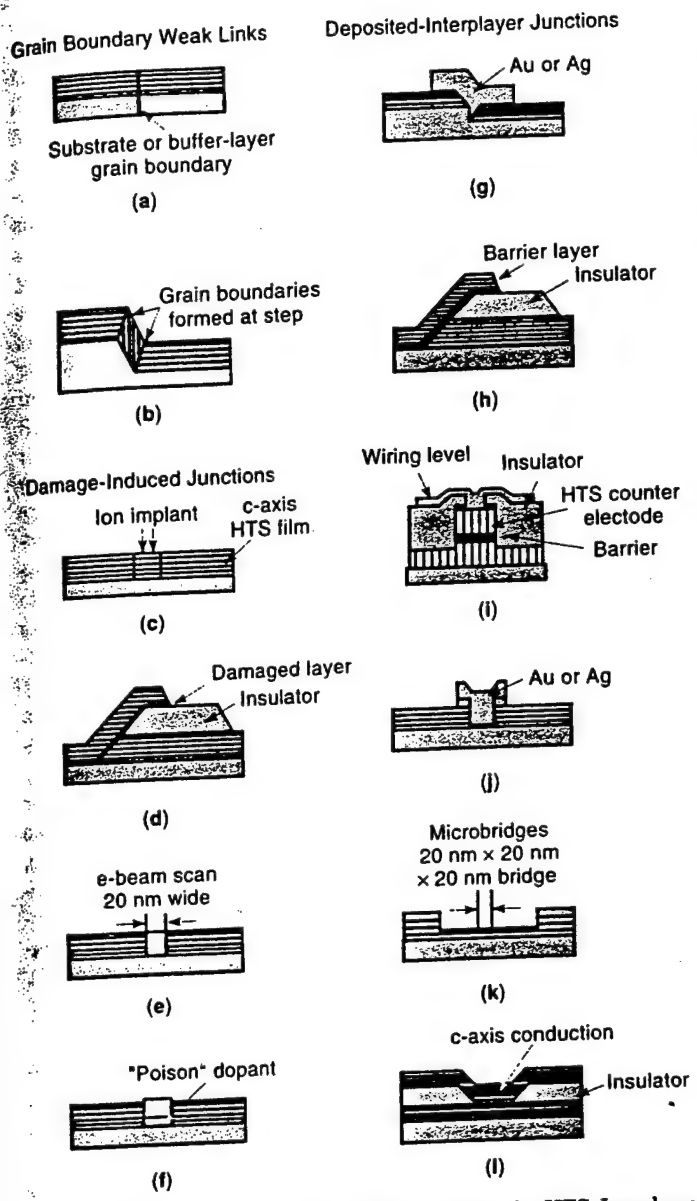

Figure 2. The wide range of fabrication methods for HTS Josephson junctions can be loosely grouped into four classes: grain boundary junctions, damage-induced junctions, deposited-interlayer junctions, and microbridges. The deposited-interlayer approaches are thought to be the most promising for applications requiring more than a few junctions.

The junction configurations shown in Fig. 2 are grouped in the four categories of grain-boundary weak links, damage junctions, deposited interlayer junctions, and microbridges. The chronology of development was that single-HTS-film configurations that did not require special substrate treatments were explored first—for example, the junctions in Figs. 2(c), 2(f), and 2(j). These were followed by more complex processes where substrates were fabricated to promote the formation of a junction during HTS film growth as in Figs. 2(a), 2(b), and 2(g). Since the configurations in Figs. 2(d), 2(h), and 2(i) are direct analogues of LTS junctions, they were identified as candidate structures soon after discovery of HTS, but development did not begin until multilayer growth and patterning techniques were developed.

Application Requirements

The key electrical parameters of an individual junction, which determine its suitability for a given application, are principally its I_c and R_N and secondarily such parameters as capacitance C and inductance L. For applications which require many junctions, such as digital circuits, the uniformity of these parameters is of critical importance, while for sensor applications, such as superconducting quantum interference devices (SQUIDs), low intrinsic noise is a key characteristic.

For digital circuits a number of constraints dictate the range of parameters required. First, the product of I_c and a typical gate inductance L_g should be not much more than a flux quantum, $\approx 2.07 \times 10^{-15}$ Wb ($\approx$2.07 pH-mA). Since it is difficult to fabricate gates with inductance less than about 4 pH in HTS (see the section entitled "Circuit Integration"), I_c can be no more than about 0.5 mA. At the same time, I_c should be large enough that the Josephson energy, $\hbar I_c/2e$, is much larger (say by a factor of 100 to 1000) than the thermal energy, $k_B T$, otherwise there will be too many thermally induced, erroneous switching events. For operation at 40 K this dictates that I_c be greater than 0.04 mA to 0.4 mA. At the same time, the product of I_c and R_n establishes the maximum reliable operating frequency of the circuit, $2eI_cR_n/h$. For Josephson devices to be competitive, this frequency must be at least tens of gigahertz. This means that I_cR_n must be greater than approximately 0.3 mV, and R_n must be of order 1 Ω to 10 Ω. While different arguments are applied for sensor applications of SQUIDs, such as magnetometry, the resulting requirements for I_c and R_n are quite similar.

JOSEPHSON EFFECTS

The dc and ac Josephson effects introduced in the section entitled "Introduction to Josephson Junctions" can be stated mathematically as follows:

$$\theta = \theta_2 - \theta_1 \tag{1a}$$

$$I = I_c \sin(\theta) \tag{1b}$$

$$V = \frac{h}{2e}\frac{d\theta}{dt} \tag{1c}$$

where θ_1 and θ_2 are the phases of the wavefunction in the two electrodes. In the presence of a magnetic field, with vector potential A, Eq. (1a) is generalized as follows:

$$\theta = \theta_2 - \theta_1 + \frac{2e}{\hbar}\int_1^2 \vec{A}\cdot\vec{dl} \tag{1d}$$

where θ_1 and θ_2 refer to two specific points on opposite electrodes, and the integral is taken along a straight line between those two points (1). While the phase difference across the junction cannot be directly measured, Josephson's predictions have several measurable consequences. For example, as a result of the periodic dependence of supercurrent on phase difference, and the field-dependence of the phase difference given by Eq. (1d), the critical current of a spatially extended junction displays a dependence on the magnetic field described by the Fraunhofer pattern characteristic of single-slit diffraction in optics: $I_c \propto |\sin(\Phi/\Phi_0)/\Phi|$, where Φ is the magnetic flux through the junction and $\Phi_0 = h/2e$ is the superconducting flux quantum. The ac Josephson effect is responsible

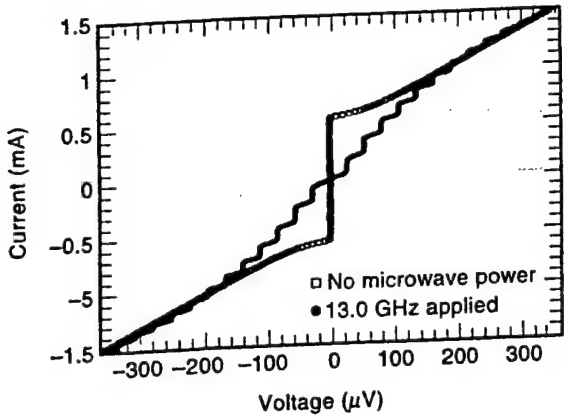

Figure 3. Current–voltage characteristics of a YBCO/Co–YBCO/YBCO edge SNS junction, showing Shapiro steps in response to 13 GHz radiation. Such steps are a manifestation of the ac Josephson effect.

for Shapiro steps, which are constant voltage steps in the I–V characteristics of the junction in the presence of microwave radiation. Such steps occur when the average voltage across the junction has values such that the oscillation frequency of the supercurrent is a multiple of the frequency of the applied radiation. This effect is the basis for the definition of the standard volt, which uses a precisely known frequency to generate a fixed voltage across a series array of many junctions. Figure 3 shows an example of Shapiro steps induced in a YBCO/Cobalt-YBCO/YBCO edge superconductor/normal metal/superconductor (SNS) junction (see the section entitled "Edge-Geometry Weak Links") by 13 GHz radiation.

Real Josephson junctions can be modeled by the so-called resistively and capacitively shunted junction (RCSJ, or, for small capacitance, just RSJ) model, which takes the ideal Josephson element described by Eq. (2) and shunts it with a resistor and a capacitor. The resistor models the path by which quasiparticles cross the junction. For HTS junctions we can use the RSJ model with a linear resistor and zero capacitance for comparison with the data. In this case the RSJ model, without thermal noise, predicts a hyperbolic shape for the I–V characteristic:

$$V = 0 \quad \text{for } I < I_c$$
$$V = R_n\sqrt{I^2 - I_c^2} \quad \text{for } I > I_c \qquad (2)$$

where V is the time average of the instantaneous voltage, $V(t)$, which oscillates at the Josephson frequency with amplitude I_cR_n. The dc behavior is illustrated in Fig. 1. In the presence of thermal noise the sharp voltage onset at I_c is smeared out.

HTS JOSEPHSON JUNCTION TYPES

As described in the section entitled "Survey of Junction Configurations," there are a wide variety of HTS Josephson junctions. In fact, it has proven relatively easy to fabricate HTS devices which exhibit Josephson effects, with the technology ranging in sophistication from naturally occurring grain boundary weak links to all-epitaxial structures incorporating superconductors, insulators, and deposited interlayers. However, it has proven difficult to meet the requirements of some of the more demanding applications. For example, single flux quantum (SFQ) digital circuits require junctions with high resistance, high I_cR_n products, and $1-\sigma$ I_c spreads less than 10%. No junction technology to date has consistently met these constraints. At present the most widely used HTS junctions are grain boundary weak links and SNS edge junctions with doped YBCO interlayers. The grain boundary devices have excellent characteristics but relatively poor I_c spreads, while the SNS edge junctions are more difficult to produce but appear to be the most viable candidate for fabrication of complex circuits.

Grain Boundary Junctions

Naturally Occurring Grain Boundary Junctions. Within a few months of the discovery of YBCO, Josephson effects were measured in bulk ceramic samples. An example of these measurements can be found in Robbes et al. (2), where a polycrystalline ceramic pellet was bonded to a glass slide, polished to a thickness of 0.25 mm, and constrictions were engraved to pattern a dc SQUID. Shapiro steps and modulation of the critical current by a magnetic field were observed.

Although randomly oriented grain boundary junctions in polycrystalline material are too poorly controlled to be practical for electronics, they are the most important obstacle in fabrication of HTS conductors for carrying large currents for large-scale, high-power applications. Many of the possible mechanisms for weak link formation at grain boundaries, such as impurities or second phase formation, have been eliminated by careful synthesis. However, the grain boundary continues to be the subject of research on topics such as the relationship between local strain fields and oxygen deficiency (3).

Bicrystal Grain Boundary Junctions. Dimos et al. (4) were the first to fabricate grain boundaries in HTS materials with controlled angles of misalignment. They cut and polished bulk $SrTiO_3$ single crystals with symmetric [100] tilt boundaries. The two crystals were sintered together with parallel [001] axes. The bicrystal was then cut and polished to obtain [001] surfaces for growth of epitaxial c-axis-oriented YBCO films. At least on a macroscopic scale, the misorientation angle in the basal plane of YBCO matched the misorientation angle in the $SrTiO_3$ bicrystal.

The bicrystal experiments elegantly quantified the need for biaxial alignment in YBCO high-current conductors by demonstrating the rapid decrease in J_c with increasing grain misalignment. They also provided a route for synthesis of grain boundary junctions, so-called bicrystal junctions, with controlled misalignment between grains and controlled placement of junctions along a single line. Strontium titanate bicrystals with 24° and 37° tilt rotations—angles where particularly well-defined, clean interfaces can be formed—are commercially available.

Bicrystal junctions are still in use for low-junction-count applications, usually where an integrated HTS groundplane is not required. Specifically, most commercially available dc SQUIDs are fabricated in this way. Bicrystal junctions are the simplest and least expensive way for a university laboratory to pattern a few junctions for research. However, in addition to the obvious disadvantage imposed by placement of junctions along a single line, junction uniformity has not

matched the level obtained by other junction configurations. Several different explanations for the lack of uniformity are based on the observation that the junction interface meanders along the substrate bicrystal boundary on a microscopic scale as YBCO grains overgrow the boundary from each side.

Biepitaxial Grain Boundary Junctions. Biepitaxial junctions are a variant of bicrystal junctions in which the bicrystal template for junction formation is provided not by a bulk bicrystal substrate but by the tendency of particular buffer layers to grow with different epitaxial orientations depending on the presence or absence of an intermediate "seed" layer. The first implementation was by Char et al. (5), who observed that $SrTiO_3(001)$ grew on *R*-plane sapphire, $Al_2O_3(1\bar{1}02)$, when there was no seed layer with in-plane parallel directions, $SrTiO_3[110]//Al_2O_3[11\bar{2}0]$. However, when there was an MgO(001) seed layer present, the in-plane orientation was $SrTiO_3[100]//MgO[100]//Al_2O_3[11\bar{2}0]$. So, by patterning the MgO layer with conventional lithography, 45° grain boundaries in the $SrTiO_3(001)$ buffer layer could be placed in arbitrary positions.

Other combinations of substrates, seed layers, and buffer layers were later found to work. All of them had in common with the original concept that the materials were oxides with dissimilar crystal structures and large lattice mismatches so that $\sqrt{2}$ times one lattice constant provided as close a match with a 45° in-plane rotation as could be achieved by cube-on-cube growth. While the virtue of this technique compared to bicrystal junctions is the ability to arbitrarily place grain boundary junctions on a mask, its disadvantage is that 45° is larger than the angle normally selected for bicrystal junctions. At this large angle, I_cR_n products at 77 K were on the order of just 10 μV to 20 μV and critical currents per unit junction width approximately 3 μA/μm. Although some multilayer SQUIDs have been based on biepitaxial junctions, there has been little work on their integration with an HTS groundplane for digital circuits.

Step-Edge Grain Boundary Junctions. When a *c*-axis YBCO film is grown over a sharp step in a cubic (or nearly cubic) substrate or deposited insulator, the YBCO grows such that the *c*-axis is perpendicular to the *local* principal crystalline axes of the substrate material (6), forming a pair of grain boundaries (at the top and bottom of the step), which behave electrically as one or two Josephson junctions. Figure 2(b) shows the simplest example, where each grain boundary (GB) is of the symmetric, (103)(103) type. Figure 4 shows a transmission electron micrograph of a cross section of such a boundary, formed at the top of a step in a single-crystal $LaAlO_3$ substrate. In practice the lower GB often consists of a mixture of orientations, including (010)(001).

Such devices show *I–V* characteristics with rather ideal RSJ shape, and they also show the signatures of true Josephson behavior, including critical current modulation with field (though often nonideal), Shapiro steps, and the emission of Josephson radiation. Values of J_c are fortuitously close to those required for digital and SQUID applications in the 65 K to 77 K range, with I_cR_n values of up to several hundred microvolts at 77 K (7). Electrical characteristics, and stability with thermal cycling, are improved by paying close attention to forming a sharp, clean step—for example, by the use of ion milling with a very hard mask, such as amorphous carbon.

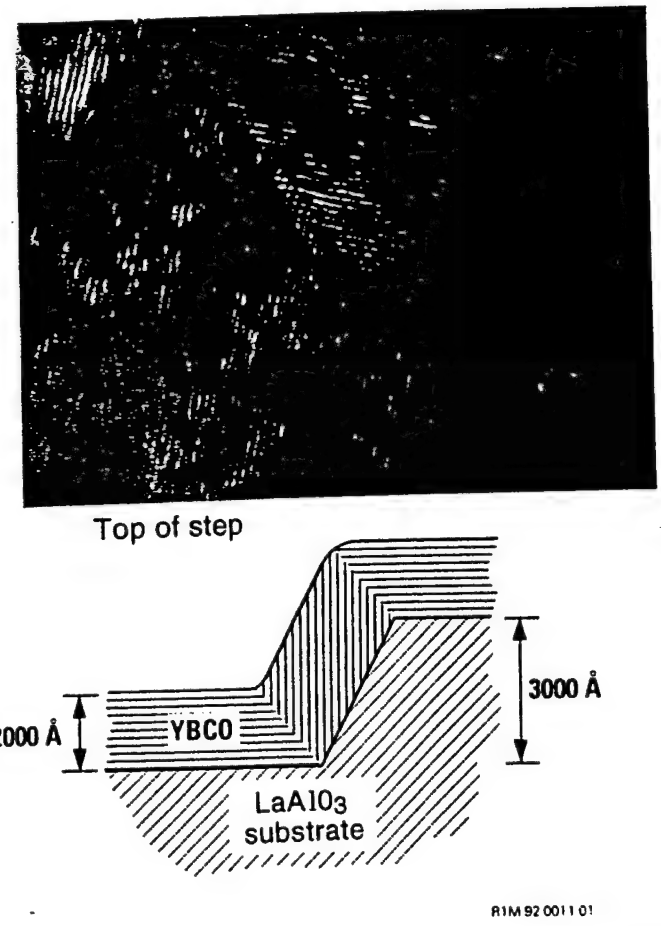

Figure 4. TEM cross-section of the upper, symmetric grain boundary in a step-edge grain boundary junction formed at a step in a $LaAlO_3$ substrate. (Courtesy of Claire Pettiette-Hall of TRW.)

While there have been reports of sets of such junctions with J_c spreads as narrow as 5% ($1-\sigma$), typical spread values are 30% or above, making the long-term viability of this junction technique for complex circuits doubtful. For SQUIDs this is not an issue; and the simplicity of fabrication, along with the low measured noise of such junctions, makes them attractive. Their incorporation into multilayers is relatively straightforward.

The nature of the Josephson junction in this geometry is controversial. For example, GBs similar to those observed in step edge junctions have been deliberately fabricated in planar YBCO films, by the use of seed layers to control film orientation (see the section entitled "Biepitaxial Grain Boundary Junctions"), and have been found to *not* exhibit weak link behavior. Also, while some of the most definitive work on these junctions has attributed the weak link to a (010)(001) GB at the bottom of the step (6), recent measurements which probe the GBs individually (by use of a narrow YBCO lead, formed by shadowing, along the step face) suggest that it is the symmetric GB at the *top* which is the weakest.

Damage-Induced HTS Josephson Junctions

Ion-Damaged Weak Links. Weak links based on ion damage can be classed into two categories: (i) single-layer devices in which a focused ion beam (FIB) creates a weak link [Fig. 2(c)]; and (ii) multilayer structures where ion surface damage of a base electrode produces a Josephson junction after deposition of a counterelectrode [Fig. 2(d)]. FIB junctions have been produced by a number of groups including Zani et al. (8), who used a 300 keV Si ion beam. The main attraction of the FIB approach is its relative simplicity, since only a single HTS film is required. However, because the typical FIB spot size is much greater than HTS coherence lengths, weak link behavior in these devices is presumably due to local variations in damage which lead to a parallel array of filamentary connections across the damaged region. Consequently, FIB-defined weak links often show nonideal I–V characteristics, as well as excess SQUID inductance. While this technology has produced high-resistance junctions and working SQUIDs up to 60 K, it has been largely superseded by other junction processes.

The second type of HTS Josephson junctions based on ion damage rely on ion bombardment at relatively low energies to create surface damage on a base electrode, which is then overlayed by an epitaxial counterelectrode. Work in this area has included room-temperature oxygen–argon and oxygen–fluorine-based plasma treatments (9), as well as low-energy Ar and Xe ion mill processing (10). The surface ion damage approach avoids the complication of a deposited interlayer and has produced high-quality Josephson junctions with I_cR_n products up to 250 μV at 77 K. However, the weak links working at 77 K also typically have current densities and resistances which are not well-suited to digital and SQUID applications ($J_c > 10^5$ A/cm^2 and $R_nA < 2 \times 10^{-9}$ Ω-cm^2). More recently it has been found that radio-frequency (RF) plasma exposure at 400° to 500°C can produce higher resistance weak links with J_c 1–σ spreads as small as 8% at 4.2 K (11).

Electron-Beam-Damaged Weak Links. Electron-beam-damaged junctions are fabricated by writing a line across a narrow, 2 μm to 10 μm wide bridge with an electron beam in a transmission electron microscope with 120 keV or 350 keV beam energies (12). The electrons are thought to disorder oxygen ions located in the chains of copper and oxygen which are present in YBCO. The higher damage energy, 350 keV, results in a weak link that is stable at room temperature, whereas disorder caused by 120 keV electrons starts to heal even at room temperature. In either case, the evidence for oxygen disorder is mainly found in (a) the annealing behavior of these junctions which tends to a recovery of the initial, undamaged bridge properties over time with temperatures <400°C and (b) energy barriers of 1.1 eV which are characteristic of the chain oxygen sites.

Targeted junction properties can be achieved by adjusting the total damage dose and the junction length. Critical current modulation in a magnetic field indicates that the damage is uniform compared to the scale of the junction width. The most sophisticated digital circuit demonstrations that have been performed without integrated HTS groundplanes have used this type of junction. A possible long-term limitation of any sequential process of writing to form junctions using either electron or focused ion beams is that writing time can become significant as circuit complexity and junction counts increase. The special equipment required, the lack of junction stability, and the fact that groundplane integration has not yet been demonstrated are other probable reasons why this technique has been used in university laboratories but has not been adopted by industrial labs.

"Poisoned" Weak Links. An alternative technique for weakening a small area is to dope an HTS film with a small patch of a material that degrades the superconducting properties. In the example of Simon et al. (13), a 10 nm thick, several-micron-wide Al stripe was patterned on a substrate before deposition of a 200 nm thick YBCO film. A weak link formed where a bridge patterned in the YBCO film crossed the Al stripe. The Al dopant depressed the critical current of the YBCO by two orders of magnitude.

This technique has the benefit of a simple fabrication process but has not been used in recent years. It is included here for completeness and to illustrate two of the factors that influence junction reproducibility: control of bridge length and control of interface thickness. Since the ideal length of a coupling region between YBCO banks is no greater than tens of nanometers, it is preferable that the length is determined by a reproducible scale such as a film thickness or step height rather than the width of a patterned line. The deposited interlayer junction configurations described below are designed to use these better-controlled length scales and to maintain a thinner interface layer between undamaged YBCO banks and a more weakly superconducting region than one can achieve by an interdiffusion process.

Deposited-Interlayer Josephson Junctions

Step-Edge SNS Junctions. Like the step-edge grain boundary (SEGB) junction, the step-edge SNS junction is formed at a step, either in the substrate or a deposited insulator, but in this case the deposition is performed directionally, from behind the step, so that the YBCO is discontinuous. This discontinuity is bridged by an in situ deposited noble metal such as Ag (14,15), making the nominally SNS structure illustrated in Fig. 2(g). A cross-sectional scanning electron micrograph of an actual device is shown in Fig. 5, which clearly shows the YBCO to be discontinuous across the step. In practice the resistance of such a device is dominated not by the normal metal itself, but by the interfaces with the YBCO. By using a directional ion mill from behind the step, it is possible to remove most of the normal metal, leaving only that which is shadowed by the step. In this case, R_n can be as much as 10 Ω, and I_cR_n as high as several millivolts, at 4.2 K. Useful SQUIDs operating at 77 K, with either "flip-chip" or integrated pick-up coils, are routinely fabricated, with modulation voltage of several microvolts. Statistics for large numbers of junctions are not available to evaluate the critical current spreads. The directionality of the fabrication process means that this junction type does not scale well for complex circuit fabrication.

Edge-Geometry Weak Links. The HTS edge-geometry weak link is also known as an edge junction or ramp junction and is shown in Fig. 2(h). This structure typically consists of a c-axis-oriented HTS base electrode film overlaid by a thick insulator (not necessarily epitaxial) with an edge produced in

Figure 5. Cross-sectional electron micrograph of a step-edge SNS junction of the type shown in Fig. 2(g), clearly showing the discontinuity of the YBCO film (dark) over the step, bridged by the Au–Ag alloy (light). (Courtesy of Mark DiIorio of Magnesensors Inc.)

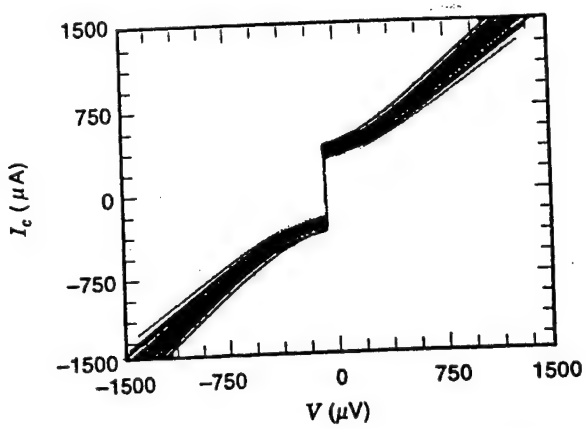

Figure 6. I–V characteristics at 65 K for a chip with junction parameters suitable for SFQ logic. There are nineteen 4 μm wide junctions with 50 Å Co-doped YBCO interlayers and an average resistance of 0.97 Ω ($1-\sigma$ = 6%). The average I_c is 327 μA ($1-\sigma$ = 13%) and the average I_cR_n product is 315 μV ($1-\sigma$ = 9%).

the bilayer by ion milling or more rarely by wet etching. An epitaxial normal metal interlayer is deposited on the exposed edge followed by growth and patterning of the HTS counterelectrode. The SNS edge junction configuration is the most widely used HTS junction approach, because this geometry offers a number of advantages, including the fact that the critical superconductor/normal metal (SN) interfaces are located on the longer-coherence-length surfaces of the superconducting electrodes. The edge structure also enables the fabrication of very-small-area devices using conventional photolithography because one of the device dimensions is determined by the thickness of the base electrode film. Not surprisingly, however, successful fabrication of uniform sets of high-quality SNS edge junctions requires great care in base electrode edge formation. Shallow edges (<40°) are needed to avoid grain boundary formation in the counterelectrod, and the edge properties must be independent of edge orientation for ease of circuit layout. The most common approach to edge formation uses argon ion milling with rotating substrates and a tapered photoresist mask. Base electrode edge cleaning before growth of the normal metal and counterelectrode is also important and is usually done by low-energy ion milling or by etching in a dilute (<1%) solution of bromine in alcohol.

As with trilayer junctions (discussed below), the edge junction approach utilizes an all-epitaxial stack of base electrode, normal metal interlayer, and counterelectrode which places tight constraints on potential interlayers. Suitable interlayers must be lattice-matched to the HTS electrodes, grow without pinholes, and be chemically compatible with the superconductors at the elevated temperatures necessary for epitaxial growth. These requirements point to the use of materials with similar structures and compositions to YBCO such as $PrBa_2Cu_3O_7$ (PBCO) or $YBaCu_{3-x}Co_xO_7$ (Co-doped YBCO) (16), the two most commonly used interlayers. Note that the interlayers are often referred to as "normal metals," but, in fact range from semiconductors (PBCO) to superconductors operating above their transition temperature (Co-doped YBCO).

I–V characteristics for a set of Co-doped YBCO edge junctions produced at Northrop Grumman are shown in Fig. 6 (17). The normal metal layer is 50 Å of $YBaCu_{2.8}Co_{0.2}O_7$. For this chip the average junction parameters, at 65 K, are J_c = 4.1×10^4 A/cm² with $1-\sigma$ = 13%, I_cR_n = 315 μV with $1-\sigma$ = 9%, and $R_nA = 7.7 \times 10^{-9}$ Ω-cm² with $1-\sigma$ = 6% (R_n = 0.97 Ω), values which are suitable for small-scale SFQ circuit applications. Note that this resistance value is surprisingly high for SNS junctions, as will be discussed in more detail in the section entitled "Advanced Issues." As shown in Fig. 7, the critical current modulation in edge-geometry weak links can approach the ideally expected $|(\sin x)/x|$ behavior, indicating fairly uniform pair current transport through the normal metal layer (17). Good results have also been obtained for junctions utilizing PBCO and Ga-doped PBCO interlayers. For example, Verhoeven et al. (18) have produced Ga-doped PBCO edge junctions with I_cR_n products up to 8 mV at 4.2 K.

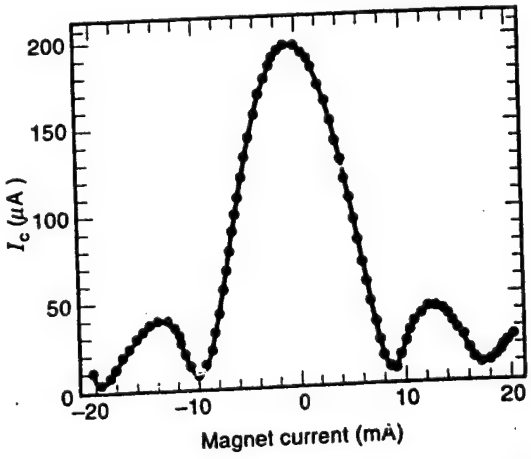

Figure 7. Critical current modulation at 55 K for a 4 μm wide SNS junction with La-YBCO base electrode, with the magnetic field normal to the substrate. The normal metal layer is 50 Å of Co-doped YBCO, and the junction resistance is 1.1 Ω.

The data suggest that transport in these devices takes place by resonant tunneling.

Trilayer-Geometry Weak Links. Trilayer-geometry Josephson junctions [Fig. 2(i)] consist of a layered sandwich structure of HTS, interlayer, and HTS epitaxial films, as well as associated wiring and insulator layers. This approach most closely resembles the highly successful LTS Nb–Al tunnel junction process and consequently has attracted considerable attention. However, the trilayer process does require additional epitaxial insulator and HTS layers for wiring. Another potential disadvantage of this approach is the relatively large area of the devices, which can lead to unacceptably low values of R_n in many SNS processes, as well as a greater sensitivity to defects such as pinholes. Some of the earliest work in HTS deposited-interlayer weak links utilized *c*-axis oriented YBCO electrodes with a PBCO interlayer (19). Researchers at Varian have used a molecular beam epitaxy approach to engineer *c*-axis trilayers on a layer-by-layer basis (20). Most recent studies of trilayer junctions have focused on *a*-axis-oriented or (103)-oriented trilayers due to the longer superconducting coherence length parallel to the *a*–*b* planes, which in principle should lead to larger I_cR_n products. While it is not clear how an *a*-axis trilayer epitaxial wiring scheme will deal with the inherently lower J_c for wiring runs along the *c*-axis direction, some promising results have been obtained with this approach. Sato et al. (21) have produced (103)-oriented trilayer junctions with 350 Å PrBaCuO interlayers that exhibit RSJ *I*–*V* characteristics at 50 K with J_c = 440 A/cm², $1-\sigma$ = 38%; $R_nA = 1.2 \times 10^{-7}$ Ω-cm², $1-\sigma$ = 21% (1.3 Ω for a 3×3 μm² junction), as well as sensible magnetic field modulation.

Planar or In-Line Junctions. These junctions, illustrated in Fig. 2(j), consist of a narrow gap (<1 μm) in a YBCO film, bridged by a normal conducting film either situated below the YBCO or deposited on top after the gap is etched by, typically, a focused ion beam. The normal layer is usually Au or Ag (above the YBCO) or PBCO (above or below). While the normal metal coherence length of Au is long enough that gaps of order 1 μm should support a critical current, the estimated values of ξ_N for PBCO and similar materials are so short that even devices as short as 0.1 μm should not exhibit a critical current. The fact that they do has been used as evidence to suggest the existence of a "long-range proximity effect" in these materials, although the existence of this is controversial. For example, it is possible that the critical current is partly due to YBCO not fully removed from the gap.

There is little data on the reproducibility of these devices, but it is generally believed that they have little potential for applications requiring many junctions. In addition, their characteristics are relatively nonideal, often exhibiting large excess current for example.

Microbridges

If a superconducting bridge is made with a width comparable to the coherence length, ξ, it behaves as a Josephson junction. Since ξ is only a few angstroms in YBCO, this is not a practical way to make a Josephson device. However, if a bridge is wider than ξ, but still less than the penetration depth λ, it can behave in many ways as a Josephson junction, for example, exhibiting constant voltage steps in response to applied microwaves, in this case as a result of magnetic field vortices moving across the bridge in synchronization with the microwave field. As such they may be useful for SQUID applications, but not for SFQ circuits.

These devices have been fabricated both in the *a*–*b* direction [Fig. 2(k)], using focused ion beam etching for example, and in the vertical direction in a *c*-axis film [Fig. 2(l)]. The latter case is interesting in that the corresponding penetration depth is long enough (~1 μm at 77 K) that conventional photolithography suffices. The *c*-axis microbridges have demonstrated encouraging I_c uniformity [13% for a few devices (22)], although critical currents are typically somewhat high, and resistances low, compared to typical application requirements, suggesting that more aggressive lithography may still be required. Low-inductance multilayer SQUIDs have been demonstrated, and the fabrication process is quite compatible with the needs of a multilayer process.

CIRCUIT INTEGRATION

Multilayer Circuit Requirements

Multilayer structures are required for many important applications of HTS junctions including digital circuits, SQUIDs with integrated pickup coils, voltage standards, and phase shifters, among others. Junction-specific requirements on I_c and R_n for some of these applications have already been discussed in the section entitled "Overview." It is desirable that these junction properties be independent of location in a multilevel structure—for example, on or off of groundplanes. This is a nontrivial constraint because junction performance is often intimately related to details of film microstructure which can be affected by growth over the underlying layers in a multifilm stack. Multilayer circuits also require good electrical isolation (>10⁴ Ω-cm) between superconducting layers, using insulators with low dielectric constants and low losses, if high-frequency applications are the objective. High-critical-current-density vias and crossovers (>10⁵ A/cm²) are essential for most HTS circuit applications. Digital circuits also call for the integration of superconducting groundplanes to produce the low-inductance SQUIDs and interconnects needed for SFQ logic. More complex circuits can require additional epitaxial insulators and wiring levels as well as integrated resistors.

Fabrication Issues

A cross-sectional schematic view of the multilayer structure used to integrate edge SNS junctions on an HTS groundplane is shown in Fig. 8. A minimum of four mask levels and six epitaxial oxide film layers are needed for this process. Additional epitaxial film layers are often used such as buffer layers between the substrate and groundplane, or passivation layers above the groundplane, but these additional layers do not alter the basic processing steps.

The substrate selected for the most complex multilayer structures is single-crystal, perovskite-structure $NdGaO_3$ which is representative of the other candidate substrates. The (110) and (001) faces of $NdGaO_3$ are virtually identical in providing a square two-dimensional lattice with approximately a 1% lattice mismatch for growth of *c*-axis-oriented epitaxial YBCO films.

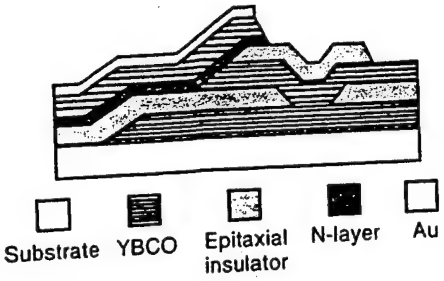

Figure 8. Schematic cross section of a multilayer process incorporating edge SNS junctions over an HTS groundplane. The horizontal shading of the YBCO layers indicates the direction of the copper–oxide planes. All layers are expitaxial except for the Au, used for contacts.

The most important requirements for YBCO groundplane films are magnetic penetration depths, $\lambda(T)$, close to intrinsic values and smooth surfaces. These properties can be achieved, in principle, by films grown by a number of different techniques. In practice, pulsed laser deposition, sputtering, and co-evaporation are the three techniques most commonly used for multilayer film growth. The effect of the penetration depth on circuit inductance is discussed in the next section. The smoothest films, those with approximately 1 nm root-mean-square (rms) roughness, have less than $10^3/cm^2$ of the outgrowths that are commonly found in YBCO films. Most of the outgrowths are second-phase copper oxide particles that are 0.5 mm to 1.0 mm in diameter and grow higher than the film surface by a distance comparable to the film thickness.

As long as a copper oxide outgrowth does not form in a location where a junction is patterned, it does not have a deleterious effect on YBCO film properties. For applications of YBCO films requiring a single layer, such as bandpass radio frequency (RF) filters, no effort is made to minimize them. In fact, their presence is a sign that excess copper available at the growing film surface has been consumed, leaving behind a matrix of stoichiometric YBCO which has optimized properties. However, outgrowth density must be minimized by a slightly copper-deficient film composition for multilayer circuits to maintain electrical isolation between layers by the epitaxial insulators.

The epitaxial insulator that grows with the best edge coverage and smoothest surfaces is $SrTiO_3$. Its high dielectric constant, on the order of $\epsilon = 500$, is not a problem for low-frequency applications such as SQUID magnetometers. However, there is no consensus materials choice at present for high-speed digital circuits where a dielectric with $\epsilon = 10$ to 30 is a practical maximum. Examples of relatively low-ϵ materials used as epitaxial insulators are Sr_2AlNbO_6 and Sr_2AlTaO_6.

Since the integration level is very low at this stage of the development of HTS circuits, demands on lithography are minimal, and this is usually performed with contact lithography and standard resists. However, to avoid formation of step-edge grain-boundary junctions where interconnects cross steps in underlying films, an etch process is required that results in sidewalls that are sloped just 5° to 30° from the plane of the substrate—similar to the angles used for edge SNS junction fabrication. Tapered edges are obtained by ion milling with Ar or Ar/O_2 mixtures with the ion beam at an angle with respect to the substrate and the substrate rotating about its normal.

Because the surface of YBCO reacts with air and photoresist to form an amorphous layer of carbonates and hydroxides 2 nm to 10 nm thick, the surface must be cleaned after lithography and before a subsequent epitaxial film layer can be grown. In the case of edge SNS junctions shown in Fig. 8, the most important exposed surface is the edge cut in the base electrode which will serve as the template for growth of an *N*-layer and YBCO counterelectrode. Some combination of oxygen plasma ashing, blanket removal of the reacted layer by ion milling, and wet chemical etching, typically with bromine–alcohol mixtures, is performed to prepare surfaces for the next film deposition.

Figure 8 shows that a Au contact layer is typically used to complete this multilayer structure. The contact layer is normally deposited in situ—that is, after the YBCO counterelectrode layer has been deposited and cooled to room temperature in oxygen, but before it has been exposed to air. In situ Au deposition lowers contact resistance and improves adhesion. Other room-temperature film layers may be required for resistors and for electrical isolation of the resistor layers, but they do not require the same care that must be taken for film layers grown at high temperature.

Groundplanes

As discussed in the section entitled "Application Requirements," digital circuits require low inductances, of order a few picohenries, to ensure that the LI_c product is about a flux quantum. The standard way to keep inductances low is to incorporate a superconducting ground plane above or below the active devices, which tends to confine the magnetic field in the relatively small volume between the two (or more) superconductor layers. Calculation of inductance is also simplified for this geometry since the problem is essentially reduced to counting squares and using the expression for the inductance per square of such a microstrip line:

$$L_{sq} = \mu_0 d\kappa \left(1 + \frac{\lambda_1}{d}\coth\left(\frac{b_1}{\lambda_1}\right) + \frac{\lambda_2}{d}\coth\left(\frac{b_2}{\lambda_2}\right)\right) \qquad (3)$$

where d is the insulator thickness, b_1 and b_2 the superconductor thicknesses, and κ is a factor that determines the field strength at the center of the finite width microstrip. The long penetration depth of YBCO, compared to Nb for example, means that the inductance per square is much higher. For example at 65 K we have $\lambda_1 = \lambda_2 = \lambda \approx 0.23$ nm, so for $d = b_1 = b_2 = 0.2$ nm and $\kappa \approx 1$, we have $L_{sq} \approx 0.84$ pH. Contrast this with the case for Nb at 4.2 K, where $\lambda \approx 0.04$ nm and $L_{sq} \approx 0.35$ pH. Thus the circuit-driven constraints of low inductance are particularly difficult to meet for HTS materials. Given the need for high I_c for thermal stability, the requirement that LI_c be about a flux quantum is particularly difficult to achieve, suggesting the need for novel gate layouts in HTS.

The integration of a YBCO groundplane has been demonstrated for several HTS junction types, including step-edge SNS, step-edge grain boundary, and edge SNS junctions. Measured inductances are consistent with other measurements of the penetration depth.

Example Circuits

The key factor in determining the yield of working HTS circuits is the degree of control over junction critical currents—especially the on-chip spread. The more complex the circuit, the tighter the I_c spread must be, although the numerical relationship between I_c spread and circuit yield depends on the circuit margins. While LTS SFQ circuits often exhibit wide margins, of order 30% or more, extrapolating such values to HTS operation at 40 K to 65 K is controversial. If these margins do hold out, possibly in cases where bit-error rate is not a driving concern, then spreads of 15% should allow, based purely on statistical arguments, yields of 50% for circuits with up to about twenty junctions (24). In fact a number of such circuits have been demonstrated at up to about 65 K, at least at low speed, bearing out some optimism.

Demonstrated HTS gates or circuits include digital devices such as logic gates (OR, AND, etc.), set-reset flip-flops, toggle flip-flops, sampling circuits, and shift registers, as well as analog devices such as SQUID amplifiers. For digital devices, in which all of the junctions need to "work" for correct operation, the highest junction count is about 30. Figure 9 shows an example of a 10-junction circuit—the first stage of a low-power analog-to-digital converter, fabricated with edge SNS junctions over a ground plane.

So far there has been very little work to quantify the experimental margins of such HTS circuits. Should the more pessimistic estimates of HTS SFQ margins be borne out, then it may be necessary to rely on voltage-state logic, where increased power dissipation will erase one of the major advantages of superconductivity, or on multi-flux-quantum schemes, several of which have been proposed.

Manufacturability of HTS circuits will also require that chip-to-chip parameter spreads be well controlled. For a single circuit it may be feasible to tune the operating temperature to, for example, adjust the average critical current to the desired value, but this is clearly not practical for a system consisting of several separately manufactured superconducting circuits. Adjustment of overall circuit biases is a more practical solution to poorly targeted critical current values but will significantly increase costs due to the need for increased circuit testing and qualification. Thus ultimately it will be necessary to control chip-to-chip parameter reproducibility to the level of a few percent at most, which will be a significant challenge for these complex materials.

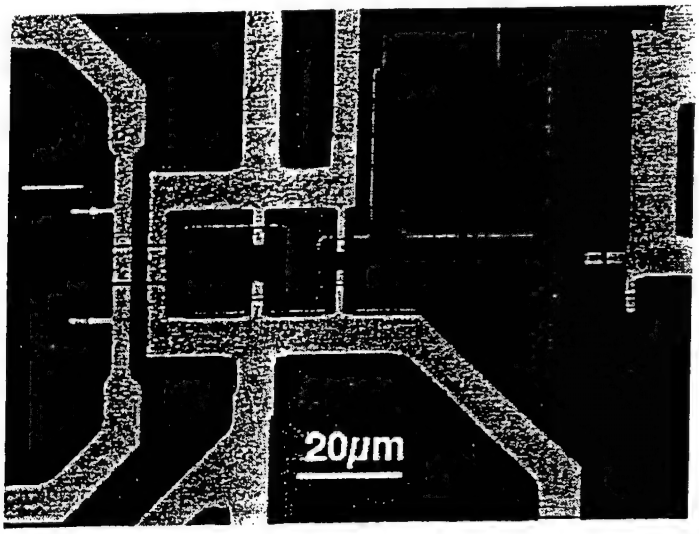

Figure 9. An example of a simple multilayer HTS circuit, a 1-bit analog-to-digital converter, fabricated with edge SNS junctions over an HTS groundplane. The lightest areas are the gold-coated counterelectrode, while the darkest are the base electrode. The process used to produce the circuit is extendible to much more complex circuits, provided that junction critical current uniformity can be improved sufficiently.

There is no single answer to the question of what is the best application for HTS Josephson junctions. However, a consensus of those working in the field believes that applications that utilize the analog precision of Josephson devices constitute the most promising niche where Josephson devices can surpass semiconductor circuits. Thus there is an emphasis on high precision analog-to-digital and digital-to-analog converters in such applications as radar, communications, and precision instrumentation. For example, an A-to-D converter with 20 bits of accuracy on a 10 MHz signal bandwidth would leapfrog semiconductor A-to-D converters, based on their historical rate of progress, by about 10 years. A potential application of such a converter is in radar, where it is desired to pick out a small target (airplane, missile) from a large "clutter" signal (rain, mountainous terrain, waves). Such a circuit should contain, depending on the details of the architecture, anywhere from several hundred to several thousand Josephson junctions. Assuming circuit margins of 30% (which may be optimistic), the required junction critical current spread for 50% yield, based on the calculations of Ref. 23, would be approximately 10% to 8%. Should the margins be reduced to, for example, 15% due to thermal noise issues, then the required spread would be more like 5% to 4%.

The issue of operating temperature is also of crucial importance, and is influenced by the potential circuit performance, as limited by thermal noise, and the availability, reliability, size, weight, and cooling power of the cryocooler. For example, a typical Stirling-cycle cooler with 0.3 Watts of heat-lift at 4.2 K would have an input requirement of some 1500 W, and would weigh about 250 pounds. This power and weight probably rules out the application of LTS circuits in most airborne platforms. On the other hand a Stirling cooler with 4 W of heat lift at 77 K would only require about 100 W of input power, and should weigh only about 10 pounds, making airborne deployment much easier. Operating at 40 K, should thermal noise require it, might reduce the available heat lift to 0.4 W, which should still be sufficient circuits of several thousand junctions.

ADVANCED ISSUES

Proximity Effect

When a superconductor and normal metal are brought into contact, Cooper pairs from the superconductor can diffuse into the normal metal. Due to phonon-induced pair breaking, the pair amplitude (also known as the superconducting order parameter or wavefunction) in the normal metal decays exponentially over a decay length defined as the normal metal coherence length, ξ_n. In the clean limit where l_n, the mean free path in N, is much greater than ξ_n, the coherence length is given by

$$\xi_{ac} = \frac{\hbar v_n}{2\pi kT} \tag{4}$$

while in the dirty limit with $l_n \ll \xi_n$, the coherence length is

$$\xi_{nd} = \sqrt{\frac{\hbar D_n}{2\pi kT}} \tag{5}$$

where the diffusion constant, D_n equals $v_n l_n/d$ and d is the dimensionality. Theories describing the details of the superconductor–normal-metal "proximity-effect" interaction have been developed for a variety of cases including back-to-back SN contacts—that is, the SNS weak link (24,25). In the SNS Josephson junction, pairs from each superconducting electrode "leak" into the normal metal interlayer and the overlap of the exponentially decaying pair amplitudes determines the strength of interaction between the superconductors. Consequently, the magnitude of the Josephson critical current scales as $\exp[-L/\xi_n(T)]$, where L is the normal metal bridge length. More specifically, in the dirty limit for long SNS bridges ($L \gg \xi_n$) relatively close to T_c ($T > 0.3T_c$), it is found that

$$I_c(T;L) \cong \frac{\pi}{2eR_n}\frac{|\Delta_i|^2}{kT_c}\frac{L}{\xi_{nd}(T)}e^{-L/\xi_{nd}(T)} \tag{6}$$

where Δ_i is the superconducting gap at the superconductor–normal-metal interface. This equation indicates that the critical current of an SNS weak link should also vary exponentially with temperature, because of the $(T)^{-1/2}$ temperature dependence of the dirty-limit normal-metal coherence length. The exponential length and temperature dependence of the critical current are the distinguishing signatures of true proximity effect devices. Indeed, there are a number of examples of HTS SNS devices which are largely consistent with proximity effect theory, most notably the junctions using Co- or Ca-doped YBCO as the normal metal layer. An example of exponential critical current dependence on temperature for a Co-doped YBCO SNS edge junction is shown in Fig. 10, along with a proximity theory fit to the data (26). However, it is often found that HTS devices with a nominal SNS configuration do not show an exponential critical current dependence on temperature. In fact, such devices commonly exhibit a quasilinear temperature dependence, which may indicate that pinhole conduction through the normal metal is dominating the electrical characteristics (25).

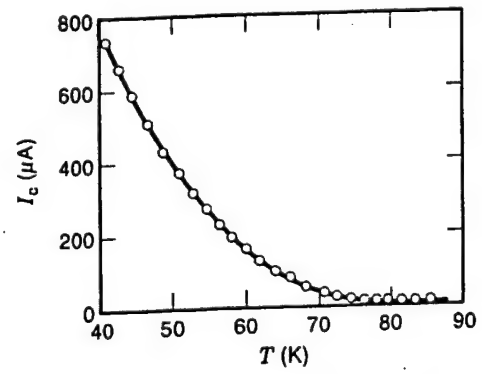

Figure 10. Critical current versus temperature for a YBCO/Co–YBCO/YBCO edge SNS junction. The solid line is a fit to the proximity effect theory of DeGennes. Despite the fact that the junction is nonideal, in that it exhibits a large interface resistance, it still appears to exhibit behavior consistent with the proximity effect.

Control of Resistance in SNS Devices

The normal state resistance of an SNS weak link is given by the sum of the normal metal resistance plus the resistance of each of the two SN interfaces. In the "ideal" SNS device the interface resistances are zero and the total device resistance is just $R_n = \rho_n L/A$, where ρ_n is the normal metal resistivity, L is the normal metal thickness, and A is the cross-sectional area. For typical values of these parameters in an SNS edge junction with a $YBa_2Cu_{2.8}Co_{0.2}O_7$ normal metal layer at 65 K ($\rho_n = 250\ \mu\Omega$-cm, $L = 100$ Å, and $A = 4 \times 0.2\ \mu m^2$) we find $R_n = 0.03\ \Omega$. In practice, such low values of resistance are often undesirable. For example, for SFQ digital applications at 65 K junctions are biased at a fixed current of order 500 μA so that the available I_cR_n product with $R_n = 0.03\ \Omega$ is only 15 μV, far less than the required value of approximately 300 μV. Increasing SNS device resistance without degrading the inherent I_cR_n product. In principle, this can be done in at least two ways: (1) by incorporating an inhomogeneous interface resistance to reduce the effective device area or (2) by producing a thin insulator at one SN interface to form an SINS structure. In practice, different groups have seen widely varying values of SNS resistance, ranging from the ideal but impractical case of very low R_nA (16) to the more technologically interesting case of high-R_nA devices (27).

For SNS weak links using Co-YBCO as the normal metal, it has been found that the interface resistance is sensitive to a variety of factors including the base electrode material and the normal metal and counterelectrode deposition conditions (17). For example, SNS devices using $YBa_2Cu_3O_7$ base electrodes grown by pulsed laser deposition (PLD) exhibit more than an order of magnitude lower resistance than devices with La-doped YBCO base electrodes ($YBa_{1.95}La_{0.05}Cu_3O_7$), or $GdBa_2Cu_3O_7$ or $NdBa_2Cu_3O_7$ base electrodes. Varying the normal metal and counterelectrode growth parameters can also have a dramatic effect on device resistance: High-pressure PLD growth in an $Ar-O_2$ atmosphere results in R_nA products over a factor of 10 smaller than for devices produced using the more conventional PLD deposition conditions in a pure oxygen background. While the detailed nature of the interface resistance is not understood at this point, the base electrode material dependence suggests that cation disorder (e.g., Y and Ba exchange) is affecting device resistance. The fact that the growth conditions of the normal metal also have a strong effect on SNS resistance indicates that defects "frozen in" in the early stages of normal metal growth may also play an important role in determining interface resistances. Because SNS interface resistances are strongly affected by a number of material and fabrication parameters, it is possible to control SNS device resistances over two to three orders of magnitude, with R_nA products ranging from 0.03 Ω-μm^2 to more than 10 Ω-μm^2. Importantly, even in the relatively high R_nA limit required for SFQ applications (0.5 Ω-μm^2 to 2 Ω-μm^2), Co-doped YBCO SNS devices incorporating significant interface resistance still behave like true proximity effect devices

(see, for example, Fig. 10) with parameter uniformity suitable for small-scale SFQ circuits.

Limits on Reproducibility

Speculation on the origins of parameter spreads have led to many experiments in fabrication of edge SNS junctions. Surprisingly, the fabrication parameters which result in junction resistances greater than $R_n = \rho_n L/A$ do not appear to systematically contribute to larger spreads in critical currents or other junction parameters. Similarly, the uniformity of current flow through a junction which can be inferred from $I_c(B)$ indicates that junctions with significant interface resistance maintain uniform current distributions.

Poor control over many fabrication parameters will certainly result in junction spreads worse than the state of the art. A good example is the roughness of YBCO base electrodes which gets transferred into the edge by patterning with Ar ion milling. While improvements from 10 nm to 2 nm rms surface roughness provide a measurable benefit for junction reproducibility, further improvements in smoothness have had a negligible effect. A second example is that junctions facing in all four in-plane directions sometimes exhibit a distribution of critical currents that is direction-dependent. However, when all processing steps are made isotropic, state-of-the-art junction uniformity can be achieved as easily in a set of junctions facing in four directions as in a set facing just one way.

These results have led us to examine defects that are intrinsic to YBCO. The role of oxygen disorder in YBCO has been investigated in several types of edge junction experiments. Decreasing the number of oxygen vacancies by plasma oxidation or annealing in ozone simply scales I_c for all treated junctions by a constant factor as large as five. Experiments in which orthorhombic YBCO electrodes were replaced by doped YBCO compounds which were tetragonal have been inconclusive in determining the possible role that twinning in YBCO might have on parameter spreads. Junctions were fabricated to face in ⟨110⟩ in-plane directions instead of the standard ⟨100⟩ directions to minimize the effects attributable to twinning, but no improvement in junction uniformity was observed.

Finally, the fact that similar best-case critical current spreads are observed for different junction fabrication processes using the same base electrode materials suggests that microstructural defects in the base electrode or base electrode edge are limiting I_c spreads. Further improvements in materials quality and edge formation techniques are expected to lead to improved junction spreads.

CONCLUSIONS

Josephson junctions based on YBCO are the fundamental building blocks for a variety of superconducting electronics applications operating at temperatures >50 K. The properties of individual junctions fabricated in a variety of configurations are sufficiently close to ideal Josephson behavior to meet application requirements. However, integration of junctions into multilayer circuits and demands on reproducibility of junction parameters when higher junction counts are needed have narrowed development efforts to a few promising configurations. Most of the current HTS circuit fabrication effort in industrial laboratories is based on edge SNS junctions which have been used for the most sophisticated and extendible digital circuit demonstrations. Further incremental improvements in the uniformity of these junctions to $1-\sigma$ I_c spreads less than 10% will permit medium-scale integrated circuit fabrication. A parallel effort, mainly by university researchers, is exploring higher-risk alternative junction configurations intended to circumvent some of the limitations to junction uniformity that may exist for edge junctions.

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HUMAN CENTERED DESIGN

This article is concerned with designing products and systems using a methodology called *human-centered design* (1,2). Human-centered design is a process of ensuring that the concerns, values, and perceptions of all stakeholders in a design effort are considered and balanced. Stakeholders include users, customers, evaluators, regulators, service personnel, and so on.

Human-centered design can be contrasted with user-centered design (3–6). The user is a very important stakeholder in design, often the primary stakeholder. However, the success of a product or system is usually strongly influenced by other players in the process of design, development, fielding, and ongoing use of products and systems. Human-centered design is concerned with the full range of stakeholders.

Considering and balancing the concerns, values, and perceptions of such a broad range of people presents difficult challenges. Ad hoc approaches do not consistently work—too much drops through the cracks. A systematic framework, which is comprehensive but also relatively easy to employ, is necessary for human-centered design to be practical. This article presents such a framework.

DESIGN OBJECTIVES

There are three primary objectives within human-centered design. These objectives should drive much of designers' thinking, particularly in the earlier stages of design. Discussions in later sections illustrate the substantial impact of focusing on these three objectives.

The first objective of human-centered design is that it should *enhance human abilities.* This dictates that humans' abilitites in the roles of interest be identified, understood, and cultivated. For example, people tend to have excellent pattern recognition abilities. Design should take advantage of these abilities, for instance, by using displays of information that enable users to respond on a pattern recognition basis rather than requiring more analytical evaluation of the information.

The second objective is that human-centered design should help *overcome human limitations.* This requires that limitations be identified and appropriate compensatory mechanisms be devised. A good illustration of a human limitation is the proclivity to make errors. Humans are fairly flexible information processors—an important ability—but this flexibility can lead to "innovations" that are erroneous in the sense that undesirable consequences are likely to occur.

One way of dealing with this problem is to eliminate innovations, perhaps via interlocks and rigid procedures. However, this is akin to throwing out the baby with the bath water. Instead, mechanisms are needed to compensate for undesirable consequences without precluding innovations. Such mechanisms represent a human-centered approach to overcoming the human limitation of occasional erroneous performance.

The third objective of human-centered design is that it should *foster human acceptance.* This dictates that stakeholders' preferences and concerns be explicitly considered in the design process. While users are certainly key stakeholders, there are other people who are central to the process of designing, developing, and operating a system. For example, purchasers or customers are important stakeholders who often are not users. The interests of these stakeholders also have to be considered to foster acceptance by all the humans involved.

DESIGN ISSUES

This article presents an overall framework and systematic methodology for pursuing the above three objectives of human-centered design. There are four design issues of particular concern within this framework.

The first concern is *formulating the right problem*—making sure that system objectives and requirements are right. All too often, these issues are dealt with much too quickly. There is a natural tendency to "get on with it," which can have enormous negative consequences when requirements are later found to be inadequate or inappropriate.

The second issue is *designing an appropriate solution.* All well-engineered solutions are *not* necessarily appropriate. Considering the three objectives of human-centered design, as well as the broader context within which systems typically operate, it is apparent that the excellence of the technical attributes of a design are necessary but not sufficient to ensure that the system design is appropriate and successful.

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Analogue demonstration of a high temperature superconducting sigma–delta modulator with 27 GHz sampling

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Abstract. We have successfully fabricated and tested a high temperature superconducting (HTS) sigma–delta modulator for analogue-to-digital conversion. This is the first demonstration of a GHz sampling A-to-D in HTS. The 15-junction single-flux-quantum (SFQ) circuit, fabricated using an epitaxial multilayer HTS process with YBCO/Co-YBCO/YBCO edge junctions, was internally clocked at 27 GHz and used to convert a 5.01 MHz signal. The modulator demonstrated a spur-free dynamic range of more than 75 dB. Two-tone measurements with 5.01 MHz and 5.51 MHz signals demonstrated third-order intermodulation products to be lower than −59 dBc. Demonstration of a functional HTS modulator represents a significant milestone in the development of high dynamic range ADCs suitable for such applications as surveillance radar.

1. Introduction

The sigma–delta (Σ–Δ) architecture is the preferred approach to high dynamic range A-to-D converters [1]. This oversampling approach is used in audio applications where signals at kHz frequencies are sampled at MHz by a Σ–Δ modulator, and the resulting bit stream digitally filtered, to provide resolution of 18–20 bits. Superconducting digital logic working at GHz clock speeds can potentially be applied to the conversion of 10–20 MHz signals. Realization of such a circuit in HTS technology will allow this performance while using a relatively compact, reliable, cryocooler, suitable for airborne and space applications. Towards this end we have fabricated a simple HTS Σ–Δ single-loop modulator, with 15 YBCO/Co-YBCO/YBCO edge junctions, in an epitaxial multilayer process utilizing three YBCO layers, two epitaxial insulators and integrated Au resistors. We have measured its performance at 35 K by inputting a 5.01 MHz signal, and sending the output bit stream into a spectrum analyser to measure the relative amplitude of the unwanted harmonics which determine the spur-free dynamic range (SFDR). With 27 GHz sampling rate we measured an SFDR of >75 dB, comparable to our previous demonstration of an LTS modulator [2]. Two-tone tests showed third-order intermodulation products to be < −59 dBc.

2. Circuit design

The schematic diagram of the modulator circuit is shown in figure 1. In this modulator, the critical junctions are J_b and

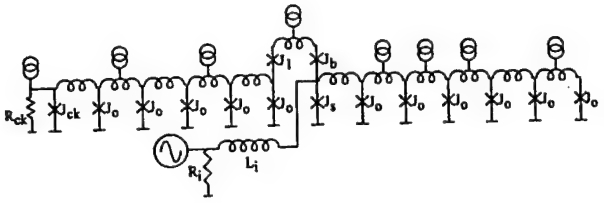

Figure 1. Schematic diagram of the designed HTS Σ–Δ modulator. Designed junction critical currents are 320 μA, except J_1 and J_b, which are 250 μA. $L_i = 20$ pH, $R_i = 10$ mΩ and $R_{ck} = 0.2$ Ω.

J_s, which perform threshold detection on the current in L_i, and, to a lesser extent, J_1, which balances the sampler when both J_b and J_s pulse in response to a clock input. Both the clock and the output were isolated from the sampling junction by a Josephson transmission line for stability. The operation of the modulator is described in [2].

The circuit was simulated using WRSPICE, and layout inductances, including junction parasitics, were extracted for comparison with design values. The fabrication process permits junctions at any angle. This design used four Cartesian orientations. Low value resistors, fabricated with interdigitated terminals, were designed using measured contact resistances.

3. Circuit fabrication

To fabricate the circuit we employed a multilayer process similar to that reported previously [3, 4], with the addition of

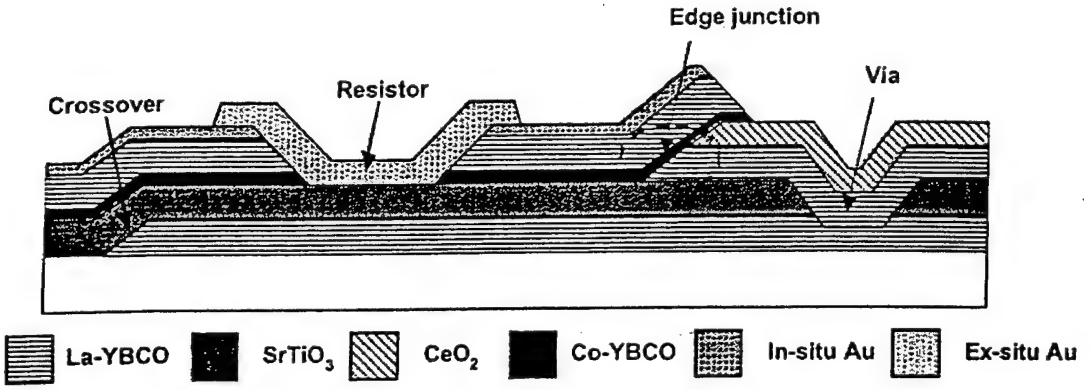

Figure 2. Schematic cross-sectional view of the HTS multilayer circuit process, illustrating key process components.

an *ex situ* gold layer to form resistors. The process, whose schematic cross-section is shown in figure 2, used pulsed laser deposition (PLD) for both YBCO and insulating $SrTiO_3$ and CeO_2 layers, with the exception of the groundplane. For this first YBCO layer we used coevaporated YBCO on an $NdGaO_3$ substrate [5] because of its low RMS roughness (typically 1.0 nm, compared to 1.5 to 2.0 for PLD YBCO). This smoothness, which is obtained somewhat at the expense of superconducting properties such as T_c and penetration depth, is found to improve targeting of the desired junction critical current (I_c) and resistance (R_n). All layers were patterned using a reflowed photoresist process (to produce tapered resist sidewalls) and angled ion milling with either pure Ar or 20% O_2 in Ar, depending on the layer and desired edge angle.

An outline of the process sequence is as follows: as-delivered coevaporated films of 225 nm thickness were patterned and etched, then cleaned using an rf oxygen plasma followed by an Ar/O_2 ion mill (our 'standard clean'). Approximately 200 nm of $SrTiO_3$ (STO) was deposited by PLD, and vias patterned by ion milling through the STO and part way into the groundplane. After another standard clean the base electrode bilayer of 200 nm $YBa_{1.95}La_{0.05}Cu_3O_x$ (La-YBCO) and 50 nm CeO_2 was deposited, patterned, and cleaned. After a wet etch in 0.3% Br in methanol a 10 nm N-layer of $YBa_2Cu_{2.80}Co_{0.20}O_x$ and a 200 nm La-YBCO counterelectrode were deposited by PLD, followed *in situ* by 100 nm of sputtered Au. The Au-coated counterelectrode was patterned by ion milling. Finally a gold resistor layer was defined by lifting off 200 nm of Au, with a Ti adhesion layer. Contact between the resistors and the La-YBCO counterelectrode was always through the *in situ* Au.

4. Process characterization

Candidate chips for circuit testing were selected by characterizing test areas within the circuit chip. This ensured that, for example, critical currents were close to the design values, and spreads were sufficiently good to give a high probability of a working circuit on that chip. These test areas included:

- 19 individual junctions of sizes representative of the circuit (3.2 and 2.5 μm wide)
- direct-injection SQUIDs to measure the inductance per square of microstrip lines
- series-arrays of base-electrode-to-groundplane vias
- series-arrays of counterelectrode–groundplane and base-electrode–groundplane crossovers
- resistors in the 10 mΩ and 0.1 Ω ranges.

The desired critical current density of 100 μA μm^{-1} (5×10^4 A cm^{-2} for 0.2 μm thick base electrodes) was obtained in the temperature range of 35 to 40 K. Thus circuits were tested in that temperature range. Junction I–V curves were RSJ-like but with a few μA of hysteresis. Typical junction R_nA products were 1.4 Ω μm^2, yielding $R_n \approx 2.1$ Ω for a 3.2 μm wide junction. We have found that junctions significantly above 1 Ω tend to have wider critical current spreads than desired—typically 20–30% (one sigma), which is inferior to our best values of 10–12%. Such wide spreads are not a major problem for this modulator since it has only one critical junction pair.

Measured microstrip inductances were 0.8 pH sq^{-1} and 1.2 pH sq^{-1} for base-electrode-over-groundplane and counterelectrode-over-groundplane, respectively. Since the latter configuration dominates the circuit the agreement with the design value of 1.5 pH sq^{-1} (which had anticipated higher temperature operation) was sufficient.

Critical currents of vias and crossovers were of the order of several mA for temperatures below about 65 K, and thus did not limit the application of the desired biases of hundreds of μA.

The Au-YBCO contact resistivity was measured to be about 5×10^{-8} Ω cm^2. This value is high enough that the nominal 10 mΩ input resistor is dominated by contact resistance rather than the resistance of the *ex situ* Au layer.

5. Circuit measurements

The measurements performed on this HTS circuit are essentially the same as previously reported for a Nb-based Σ–Δ modulator [2], except for those which required a latching amplifier, which was readily fabricated in Nb technology but not in HTS. A stable 5.01 MHz oscillator was used as a signal source. The output of this oscillator was low pass filtered to insure that harmonics present in the signal were below −90 dBc. Signal amplitude was controlled with a key-switched resistive attenuator. The clock frequency was

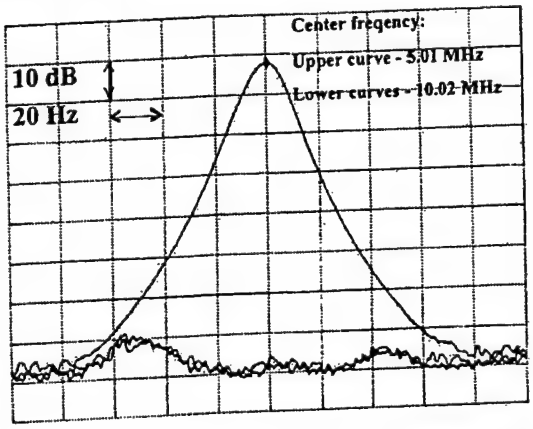

Figure 3. Spectral response of the HTS Σ–Δ modulator. The upper curve, centred at 5.01 MHz, is the output at the signal frequency. The lower curves, centred at 10.02 MHz, show the absence of harmonic response from the modulator above the noise floor of the spectrum analyser.

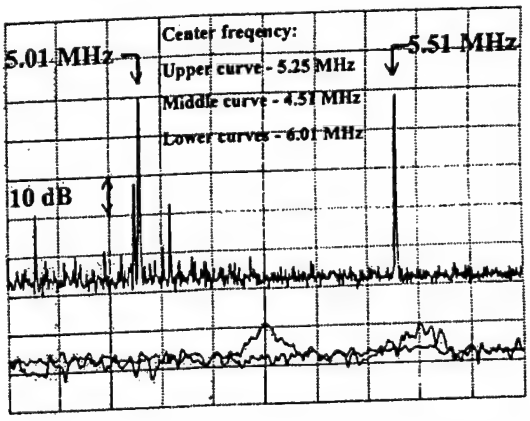

Figure 4. Third-order intermod test of the HTS modulator. The upper curve shows the two input signals at 5.01 and 5.51 MHz, with 100 kHz/division scale and 1 kHz resolution bandwidth. The middle (lower) curve, centred at 4.51 MHz (6.01 MHz) was measured at 10 Hz resolution bandwidth and expanded to a scale of 10 Hz/division to increase sensitivity. The small responses in the lower curves are within the distortion spec of the spectrum analyser.

controlled at 27 GHz by a dc current applied to the 0.2 Ω clock resistor, R_{ck}, in parallel with the clock junction, and was measured by using the Josephson voltage to frequency relation: $f = V/\Phi_0$. A dc offset current, applied to the signal input of the modulator, insured a positive voltage at the integrator.

A Hewlett–Packard 72109A spectrum analyser was used to display the spectral output of the modulator. The output signal was measured at 5.01 MHz and at 10.02 MHz using 10 Hz resolution bandwidth for maximum sensitivity. The results of this measurement are shown in figure 3. The upper curve shows the reproduction of the input signal at 5.01 MHz. The lower curves, centred at 10.02 MHz, show the response at the first harmonic, with and without an input signal. Down to the noise floor of the spectrum analyser there is no evidence of a harmonic. The small observed structure, independent of the presence of an input signal, is thought to be due to external interference. By mis-adjusting the circuit biases it was easy to bring the 10.02 MHz harmonic well into range. Biases were optimized to bring the harmonic below the noise floor.

Further evidence of the modulator linearity was obtained by measurement of third-order intermodulation products. Signal sources at $f_1 = 5.01$ MHz and $f_2 = 5.51$ MHz were combined with a power combiner. Six dB of attenuation of each port of the power combiner isolated the signal sources from each other. Signal levels were adjusted to yield output peaks 6 dB lower than the signal of figure 3, as measured by the spectrum analyser. Note that this represents the same peak-to-peak voltage swing as in the previous measurement. The output was measured at 6.01 MHz ($2f_2 - f_1$) and 4.51 MHz ($2f_1 - f_2$). In the latter case, an intermodulation product was visible at a level of approximately −59 dBc.

6. Conclusions

We have demonstrated, for the first time, an HTS Σ–Δ modulator, fabricated with an extendible multilayer process. The circuit was operated at 27 GHz clock frequency, and demonstrated a spur-free dynamic range of >75 dB, and third-order intermodulation products less than −59 dBc. Extension of the circuit to higher frequencies, and the use of a more complex double-loop modulator architecture, will take full advantage of the high speed and quantum accuracy of superconducting digital circuits, and should result in ADCs with 18–20 bits of SFDR on a 20 MHz signal bandwidth.

Acknowledgments

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Oxidation of Multilayer HTS Digital Circuits

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Abstract — **The issue of oxygen diffusion through insulating layers to buried superconductor films is common to any multilayer structure based on YBCO. Our earliest technique for obtaining fully oxidized underlayers on a practical time scale used reduced growth temperatures for strontium titanate insulating films to introduce defects which enabled oxygen diffusion while maintaining the integrity of electrical isolation. Since this approach did not work well with Sr-Al-Ta-O (SAT) and Sr-Al-Nb-O (SAN) insulators which have more desirable dielectric properties, a plasma oxidation process was introduced. For digital circuits based on HTS Josephson junctions where buried groundplanes must be fully oxidized, plasma oxidation had profound effects on the properties of cobalt or calcium-doped YBCO films used for N-layers in SNS edge junctions, increasing junction critical currents by a factor of five. These experiments offer some insight into the role of oxygen in determining both individual junction properties and junction reproducibility. A third approach to oxidation of buried films relies on "oxygen vias" patterned in the insulating layer to permit oxygen to diffuse in the a-b plane of YBCO films instead of diffusing through the insulating layer. We designed and measured test structures which set a practical limit of 20-30 micrometers for via spacing.**

I. Introduction

Low inductances needed for Single Flux Quantum (SFQ) logic circuits are best achieved by integrating superconducting ground planes in multilayer structures with the Josephson-junction and other component layers. Whether the ground plane is above or below other circuit elements, it is necessary in YBCO-based circuits to diffuse oxygen through an epitaxial ground plane insulator film to fully re-oxidize one or more buried YBCO layers.

The need for re-oxidation of buried YBCO layers originates with these materials properties:

- The growth temperatures for YBCO and related insulator oxide films are in the range of 700-850°C.
- The equilibrium oxygen content of $YBa_2Cu_3O_x$ is high enough for the film to have a high T_c, $x > 6.85$, only for temperatures, $T < 370$-410°C in typical deposition gas partial pressures of 40-400 mtorr. Even in 1 atm of O_2, YBCO has $x \geq 6.85$ only for $T \leq 575$°C. Optimal properties for YBCO require $x \approx 6.95$. At deposition gas pressures and 1 atm O_2 annealing pressure, $x = 6.95$ only for $T < 310$-340°C and $T < 480$°C, respectively.[1]
- Even with the most favorable parameters for epitaxial insulator growth, oxygen diffusion through epitaxial insulator films is slow compared with diffusion through YBCO.[2]

Specifically, when a YBCO/insulator bilayer is heated to the growth temperature for deposition of a subsequent layer, the buried layer reaches its equilibrium oxygen content ($x << 6.85$) rapidly because out-diffusion through the epitaxial insulator is high at 700-850°C. However, in-diffusion through the insulator during cooldown is slow at $T \approx 480$°C.

The problem of re-oxidation of buried films is common to all multilayer circuits based on YBCO but is most severe in the case of digital circuits due to large areas of overlap and restrictions on the choice of insulator material. For low-frequency magnetometers, the area of crossovers can be kept small and $SrTiO_3$ (STO) is a suitable insulator. Epitaxial STO films have higher oxygen diffusion rates than the other insulators we investigated, Sr_2AlTaO_6 (SAT) and Sr_2AlNbO_6 (SAN),[2] but STO has a high dielectric constant and dielectric loss that limits its use in high-speed circuits. As multilayers are introduced in passive HTS microwave circuits, filterbanks, phase shifters, etc., similar solutions to oxidation as described here will need to be employed.

II. Straightforward Oxidation Techniques

There are significant drawbacks to the straightforward approaches to oxidation of higher temperatures, longer times, or higher oxygen pressures. As the introductory description of the oxygen phase diagram for YBCO made clear, high-temperature anneals in an atmosphere of oxygen overcome the obstacle of diffusion rates but the equilibrium oxygen composition that is achieved is too low.

The approach of using long annealing times has two drawbacks. The first is that even 80-hour anneals often fail to restore adequate superconducting properties. The second problem is that long anneals should be performed after every high-temperature film deposition – not solely after the final film layer. We have found by XPS measurements that the formation of carbonates and hydroxides at film surfaces due to exposure to air occurs more rapidly for oxygen-deficient YBCO films than for fully oxidized YBCO. Furthermore, epitaxial YBCO films grown on $SrTiO_3$(110) substrates had a thicker reaction layer than found for c-axis YBCO films grown on (001) substrates. The surface of the former films simulated the edge of a c-axis film after patterning. Reaction with air or process chemicals at the patterned edges of c-axis films is expected to have the largest negative impact on circuit performance since these edges may be used for SNS edge junction formation or for contacts in high-

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current-density vias. Therefore, a fully-oxidized film is the best choice for the ultimate formation of clean interfaces.

The drawbacks of high-oxygen-pressure anneals are also practical rather than fundamental. Examination of the phase diagram of YBCO shows that in high oxygen pressures on the order of 100 atm O_2, the equilibrium oxygen content of YBCO approaches x = 6.95 at T = 650°C where diffusion rates are relatively high. Furnaces capable of operating at this hazardous temperature and oxygen pressure range are available commercially but only for sample sizes of 1 cm^2.[3]

We employed a less straightforward technique based on insulator growth temperature for several years to successfully produce devices and simple circuits with integrated ground planes.[4] STO films were deposited by off-axis rf magnetron sputtering at relatively low temperatures in the range of 680-700°C. Measurements of capacitor leakage and oxygen diffusion rates indicated that we introduced defects which enabled oxygen diffusion while maintaining the integrity of electrical isolation.[2] The alternative approaches discussed below were investigated because the yield of this process step was too low for scaling up to more complex circuits and it was less reproducible for SAT and SAN than for STO insulators.

III. Annealing in an Oxygen Plasma

Soon after the discovery of YBCO, it was found that oxidation in a low-pressure oxygen plasma could improve film properties,[5] and add more oxygen to YBCO than could be incorporated by a 1 atm O_2 anneal [6] due to a higher activity for atomic oxygen.[7] Ockenfuss, et al. [8] were the first to use plasma oxidation to re-oxidize a YBCO film covered by an epitaxial insulator. In this section, we extend the result they obtained on YBCO/$NdGaO_3$ films to bilayers with STO, SAT, and SAN, discuss the effects of plasma oxidation on films with various compositions used in SNS edge junction fabrication, and then examine the changes in junction characteristics due to plasma oxidation.

The conditions we used were 80 W of rf power applied to a 2-inch diameter YBCO sputter target in a US, Inc. sputter source, a background gas of 1 torr O_2, and a cooling time of approximately 40 minutes. Instead of the usual 90° off-axis deposition configuration, we increased the angle to ~135° to minimize the possibility of depositing a layer of material on the film surface. For films cooled in the plasma immediately after deposition, we cooled from ~725°C to 200°C before turning off the rf power. Other samples were annealed at starting temperatures ranging from 300°C to 650°C. Changes in film properties relative to a 1 atm O_2 anneal were just as large for films that were exposed to a high temperature of 300°C as for films exposed to higher temperatures.

For dozens of samples, plasma annealing restored a sharp 85-90 K T_c to YBCO/STO bilayers in cases where we

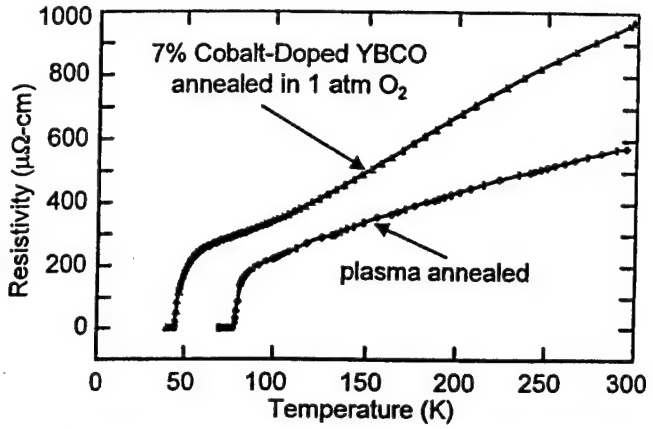

Fig. 1. Annealing in an oxygen plasma is a more effective technique for oxidation than annealing in an atmosphere of molecular oxygen. In this case of a c-axis-oriented film of $Yba_2Cu_{2.79}Co_{0.21}O_x$, resistivity was measured first after the O_2 anneal and then after a plasma oxidation. The transition temperature increased by 34 K and the resistivity at 300 K decreased by 40% – both indications of higher oxygen content.

were unable to observe a superconducting transition after annealing in 1 atm O_2 at 450°C for 2 hours and measured broad and depressed T_cs after anneals up to 80 hours long. In contrast, the same measurements performed with YBCO/SAT and YBCO/SAN bilayers yielded mixed results. In some cases, the plasma anneal still did not restore superconductivity to the buried YBCO film while a few samples were completely re-oxidized.

The results of plasma oxidation for a number of YBCO-based films that we have used for electrodes and N-layers in SNS junctions are shown in Figs. 1 and 2. Fig. 1 shows an increase in T_c and decrease in normal-state resistivity for a YBCO film doped with 7% cobalt indicating an increase in oxygen content. The $\rho(T)$ curve shifted from one that is similar to single crystals with 7% cobalt to a curve typical of 4% cobalt. A nearly identical effect has recently been reported where an ozone anneal was used instead of a

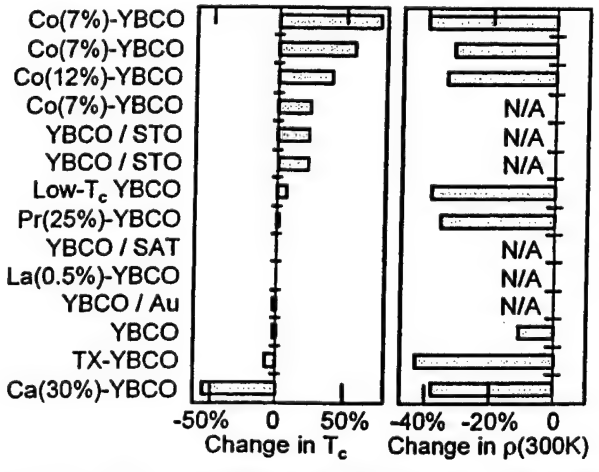

Fig. 2. The decrease in resistivity summarized here from films initially annealed in 1 atm O_2 and then plasma annealed showed that the plasma anneal adds oxygen and charge carriers. The sign of the change in T_c defines a sample as being "underdoped" or "overdoped." TX-YBCO has a composition of $Y_{0.6}Ca_{0.4}Ba_{1.6}La_{0.4}Cu_3O_x$.

plasma anneal.[9]

Fig. 2 summarizes the effects we have observed by comparing changes in T_c and ρ(300K) for every film in the first batch of samples we measured, plasma oxidized, and re-measured. In every case where contacts could be made to the underlying film, ρ(300K) decreased by 11-40%. Since the change in resistivity indicated an increase in charge carriers in every case, the change in T_c defined whether a particular sample had been "underdoped" or "overdoped." The extreme cases in Fig. 2, Co- and Ca-doped YBCO, are well known to be underdoped and overdoped, respectively.

The changes in the characteristics of SNS edge junctions due to plasma annealing are summarized in Figs. 3 and 4. The 500% increases in J_c and 50% reductions in R_n shown in Fig. 3 have several implications. First, the use of plasma annealing to oxidize an entire circuit structure will have profound effects on targeting of J_c and R_n. On the other hand, once the entire structure is oxidized, plasma oxidation can be used to tune average J_c over a wide range.

The second important observation regarding Fig. 3 is that the spreads in J_c and R_n are unaffected by plasma annealing and the ranking of specific junction parameters is nearly constant. This implies that while oxygen content strongly affects junction properties, variations in oxygen content are not the source of junction nonuniformity.

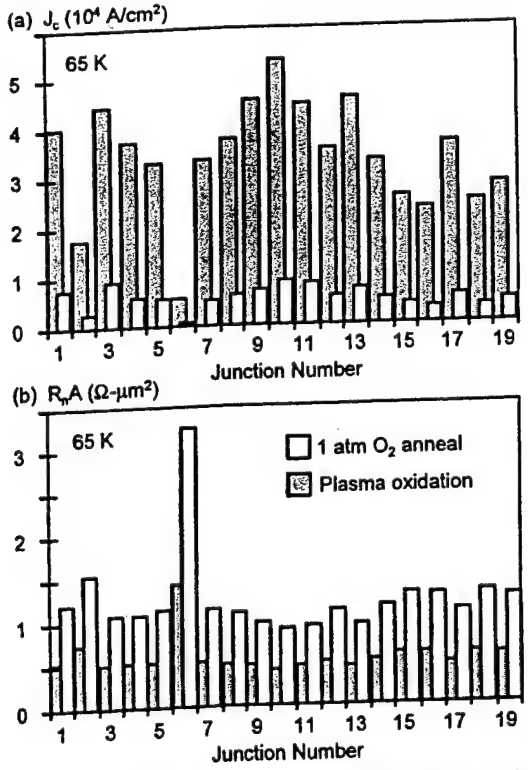

Fig. 3. Changes in J_c and R_n for a set of 19 edge SNS junctions on a single chip after plasma annealing. These junctions have La(5%)-YBCO electrodes and a 5 nm thick, Co(7%)-YBCO N-layer – all deposited by PLD. These dramatic changes indicate that it is possible to use plasma oxidation for tuning junction properties over a wide range. Other properties of these junctions can be found in Ref. 4.

The data in Fig. 3 is re-plotted in Fig. 4(a). Fig. 4(b) shows the same log-log plot for a set of junctions on a single chip which was nominally identical to the one used for (a) except for a YBCO base electrode instead of a La(5%)-YBCO base electrode. The open symbols in Fig. 4 showing junction characteristics after a 1 atm O_2 anneal are typical of our observations for roughly 200 chips which have a standard mask pattern of 19 junctions. The data points for all 200 chips tend to cluster along lines with slopes between -2 and -1. Figs. 4(a) and (b) exhibit these two extreme values for the exponent, respectively.

After plasma annealing, the two sets of data in Fig. 4 shifted along the same trend lines that relate variations in individual junction properties. This shift indicate that the fundamental mechanism for variation in junction properties – for example, variations in effective area or variations in interfacial tunnel barrier width – is unaffected by oxidation.

IV. Use of Oxygen Vias

Regardless of the effectiveness of oxygen plasma annealing for fully oxidizing multilayers with STO insulators, tuning average junction characteristics, or sorting out the possible mechanisms for junction variability, it is

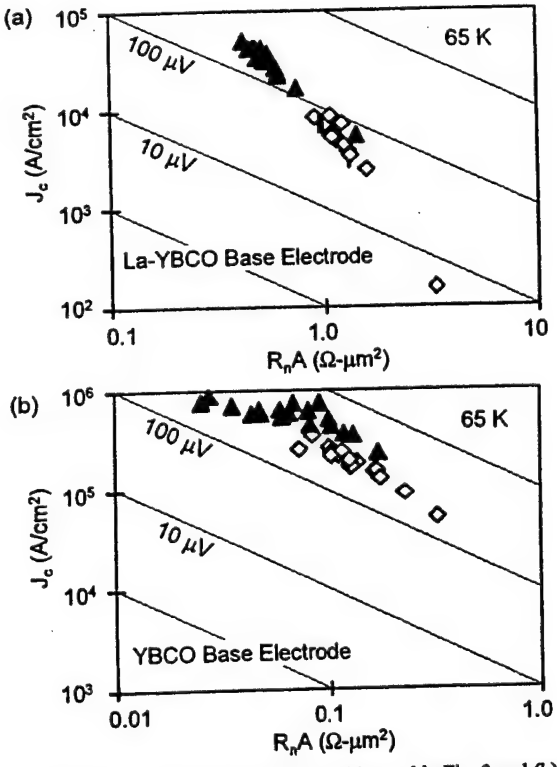

Fig. 4. Summary of J_c and R_n data for (a) the chip used in Fig. 3 and (b) a chip with a YBCO base electrode which had its N-layer and counterelectrode deposited at the same time as the chip in Fig. 3. Open symbols are for measurements after a 1 atm O_2 anneal and the solid symbols are from a second measurement after plasma oxidation. The two sets of data indicate that the fundamental mechanism for variation in junction properties – for example, variations in effective area or variations in tunnel barrier width – is unaffected by oxidation.

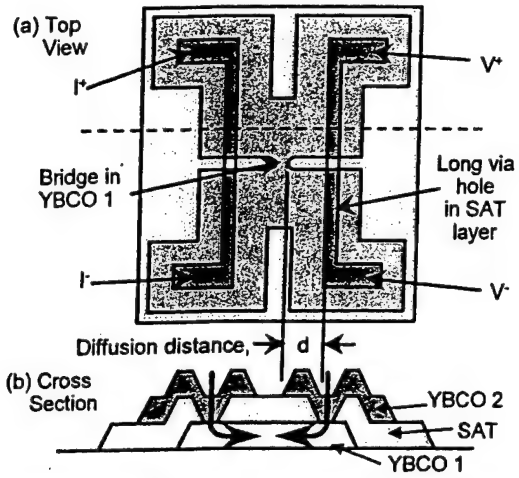

Fig. 5. Schematic views of the test structures used to measure oxygen diffusion in the a-b plane of YBCO. Oxygen ions must travel a distance, d, from via holes in the SAT insulator to the short bridge patterned in the bottom YBCO film. Each test chip had structures with values of d = 2 to 128 μm.

insufficient for oxidizing buried YBCO layers in circuits fabricated with SAT or SAN insulators.

To address these cases where insulator overlayers were impervious to oxygen diffusion, we designed the test structure shown schematically in Fig. 5 to determine whether lateral diffusion of oxygen in the a-b plane could serve as an alternate diffusion route.

The results of measurements on the lateral-diffusion test structures are shown in Fig. 6 for a chip annealed 1 hour in 1 atm O_2 at 450°C and then annealed in an oxygen plasma. Although the oxygen plasma treatment marginally improved both T_cs and J_cs, the primary conclusion from this data is that diffusion distances on the order of 10s of μm are practical. The diffusion coefficient inferred from these measurements is 7×10^{-9} cm^2/s in reasonable agreement with the value of 3×10^{-11} cm^2/s reported for the a-b plane of twinned single crystals.[10]

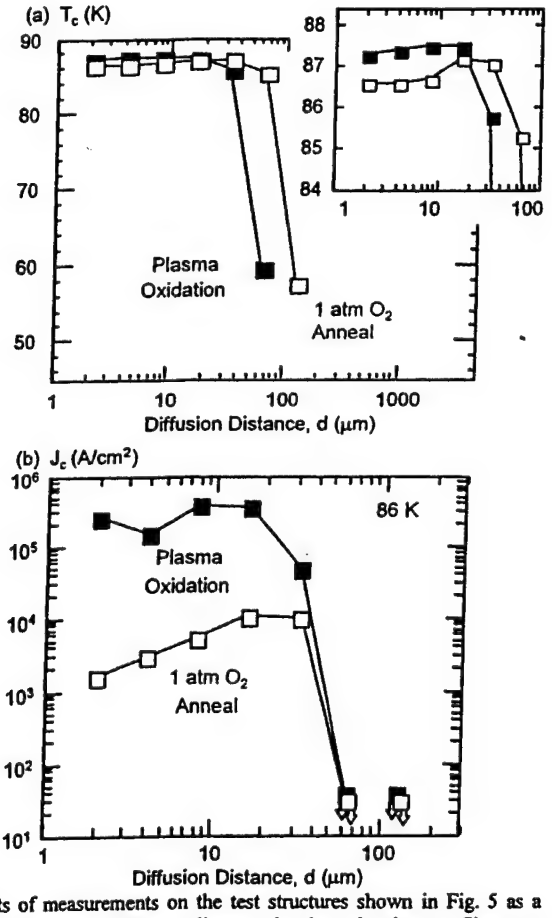

Fig. 6. Results of measurements on the test structures shown in Fig. 5 as a function of the oxygen diffusion distance in the a-b plane. Since no superconducting transition was found for long paths, the a-b plane must have been the only important path for diffusion .

V. Conclusions

The straightforward approaches to re-oxidation of buried YBCO in multilayer circuits – long annealing times, higher temperatures, and higher oxygen pressure – are impractical. Plasma oxidation is an effective approach for STO insulators which also permits tuning of average junction characteristics and serves as an aid in identifying mechanisms for junction variation. Oxygen via holes through SAT and SAN insulators are the only effective approach for these materials but vias must be spaced on the order of 10s of microns apart.

Acknowledgment

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High-Resistance HTS Edge Junctions for Digital Circuits

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Abstract—**We have investigated factors affecting the resistance of edge-geometry HTS weak links, including SNS junctions with Co-doped Y-Ba-Cu-O as a normal metal interlayer. We have also studied devices with no deposited interlayer in which the weak link is produced by ion beam surface damage or by controlled disorder near the base electrode - counterelectrode interface. For each of these weak links several parameters, including the base electrode material and the deposition conditions of the normal metal and counterelectrode, are found to have strikingly large effects on device resistance. Controlling these factors has enabled the fabrication of high-quality, high-resistance (≈1 ohm) SNS edge junctions with one-sigma I_c spreads down to 6% in 10-junction series arrays. The junctions without deposited interlayers exhibit electrical characteristics and parameter spreads approaching the best results obtained with the Co-YBCO SNS devices.**

I. Introduction

High Temperature Superconductor (HTS) digital circuits based on Single Flux Quantum (SFQ) logic require Josephson junctions with tight critical current spreads (I_c 1-σ < 10%) and normal state resistances (R_n) greater than ≈ 0.5 Ω in order to meet circuit constraints on I_cR_n products (I_cR_n > 300 μV) and critical current (I_c ≈ 500 μA at 65 K). One promising HTS junction technology uses $YBa_2Cu_{3-x}Co_xO_7$ (Co-doped YBCO) as the normal metal interlayer ("N-layer") in an edge-geometry superconductor/normal-metal/superconductor (SNS) weak link. Co-YBCO edge junctions have been successfully integrated with groundplanes[1-5], and reasonable progress has been made towards fabrication of junction chips with critical current spreads approaching the values needed for SFQ logic.

In the absence of SN interface resistance, one would predict a Co-YBCO junction resistance on the order of 30 mΩ for typical device parameters [6], more than an order of magnitude smaller than the minimum resistance required for SFQ applications. In practice, groups have seen much different values of Co-YBCO SNS resistance, ranging from the ideal but impractical case of very low R_nA [2], to the more technologically interesting case of high-R_nA, high-I_cR_n devices [1]. While the variation in Co-YBCO device resistances can be attributed to variation in interface resistances, it is important to note that the high R_nA results demonstrate that it is possible to incorporate interface resistance without significantly degrading I_cR_n products. It should also be recognized that practical values of SNS junction resistance can be obtained using more resistive interlayer materials such as $PrBa_2Cu_{3-x}O_7$ (PBCO), although interface resistance may play an important role in those devices as well.

The demonstration of high R_nA Co-YBCO junctions motivated us to examine some of the factors affecting Co-YBCO SNS resistances with the goal of understanding and controlling these variables. We found that a number of parameters can dramatically increase SNS device resistances, while preserving SFQ-compatible I_cR_n products in many cases [6]. Here we will focus on the effects of base electrode composition and growth of the normal metal and counterelectrode.

The fact that sizeable interface resistances can be incorporated in SNS edge junctions without significantly reducing I_cR_n also suggests that useful weak links might be possible *without any deposited interlayer*. Such a process would eliminate possible J_c variations due to inhomogeneities in the Co-YBCO, which could result in tighter J_c spreads. We have examined two processes without deposited interlayers. The first of these processes uses ion beam damage at elevated temperatures to form a weak link. This "hot ion damage" (HID) process was inspired in part by early work on plasma surface treatments [7,8], by studies of room-temperature ion-beam-damage junctions [9], as well as by more recent work using a high temperature Ar/O_2 plasma process [10].

The other weak link fabrication technique we have studied, which works without a deposited interlayer, utilizes direct deposition of the counterelectrode on a cleaned and sometimes chemically treated base electrode edge. Like the HID process, this technique has produced high quality, high-R_n Josephson junctions, presumably due to a small amount of crystalline disorder near the base-counterelectrode interface. We will refer to this process as the "controlled interfacial disorder" or CID process. Similarly to the Co-YBCO SNS junctions, the devices without deposited interlayers show a strong dependence on base electrode material and counterelectrode deposition. All three processes also give comparable baseline J_c spreads, which has implications for the mechanisms causing parameter variations in these weak links, as we will discuss.

II. Process Details

A. SNS Device Fabrication

Details of our SNS junction fabrication process have been given previously [1,3,4,6], but a brief overview will be presented here. The base electrode YBCO films are deposited by pulsed laser deposition (PLD) or off-axis-sputtering, and we have also used commercially-obtained coevaporated YBCO films. Our PLD-deposited base electrodes are often La-doped, ($YBa_{2-x}La_xCu_3O_7$ with x=0.025-0.075, "La_x-YBCO"), in part because a small amount of La can help suppress a-axis grain formation [3]. The base electrode edges are patterned using reflowed photoresist and 150 eV Ar ion milling at 45° with rotation, and then are typically cleaned using a sequence of an oxygen plasma, Ar/O_2 milling, and Br etching. Following edge cleaning and silver paint mounting on a substrate block, the $Co_{0.2}$-YBCO and counterelectrode are deposited and patterned

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B. Hot Ion Damage Device Fabrication

The hot ion damage process relies on using an Ar or Xe ion beam to create disorder at the base electrode surface. While room temperature ion beam damage had been used previously to fabricate high quality HTS weak links, these devices generally had resistances too low for digital applications [9]. However, the recent results from the Conductus "interface-engineered junction" (IEJ) process [10] using an Ar/O_2 rf plasma at high substrate temperatures suggested that ion bombardment at elevated temperature might be an effective way of increasing shallow surface disorder and obtaining higher R_n junctions. The IEJ process also utilizes a vacuum annealing step, which we have chosen to include in our own process to allow more direct comparison of results from the two processes.

The HID process was motivated in part by the potential benefits of an ion mill technique. The principle advantages for an ion mill vs an rf plasma process are that the lower-pressure mill technique gives a well defined beam energy with independent control of the energy and flux, while avoiding the backscattering contamination that often occurs in high pressure plasma processes. However, the the increased scattering in the plasma process also leads to more omnidirectional bombardment of the junction edges, which could result in more uniform damage and tighter J_c spreads.

The HID process starts with the same *ex-situ* cleaning procedure used for our SNS junctions. The cleaning is followed by an *in-situ* Ar or Xe ion mill treatment at 400°C at a beam energy of 100 - 300 eV with a total beam current of 5 mA in our 3 cm mill. For 200 eV Ar these conditions give a milling rate of 4-5 Å/*min* for YBCO. Typical HID milling times are 3-15 minutes. After the mill treatment a vacuum anneal is done for 30 minutes at 400°C, the heater is ramped up to the growth temperature of 790-805°C in oxygen, and the La-YBCO or YBCO counterelectrode is deposited under our standard conditions. The chips are then annealed as usual at 450-500°C in 500 T O_2.

C. Controlled Interfacial Disorder Device Fabrication

We have also developed an alternate technique for producing weak links without deposited interlayers which utilizes "naturally occurring" disorder at the base electrode - counterelectrode interface to form a Josephson junction. In this case we believe the weak link results from a combination of cation disorder in the base electrode, and disorder frozen into the initial stages of growth of the counterelectrode. As we will discuss later, the weak link parameters can be controlled by adjusting the base electrode composition and the counterelectrode growth conditions. In some variations of this process we used chemical surface treatments (CST) of the base electrode to affect the device formation.

The CID process begins with a standard cleanup followed by an optional wet chemical treatment in a nitrogen dry box with methanol solutions of Br, HF, or HCl. After transfer to the PLD system, a 350-400°C vacuum anneal is sometimes done, and then a LaYBCO or YBCO counterelectrode is deposited under normal conditions at 790 to 805°C and followed by the usual oxygen anneal.

III. Results

A. Co-YBCO SNS Junctions

In an effort to understand and control the interface resistance in Co-YBCO SNS junctions we have studied some of the factors affecting the device resistance. We found that a number of materials and process parameters have a surprisingly large impact on the resistance and I–V quality of SNS weak links. These factors include the base electrode edge angle, the base electrode material and deposition conditions, the base electrode insulator cap material, the edge cleaning technique, and the growth conditions of the normal metal and counterelectrode [6]. Here we will examine the effects of the base electrode as well as the influence of the growth conditions of the normal metal and counterelectrode, parameters which also have a major effect on the resistance of weak links fabricated without deposited interlayers.

Table I presents 77 K data for two chips with PLD-deposited base electrodes with different compositions: $La_{0.05}$-YBCO and undoped YBCO. In this case the base electrode edges were Br cleaned, which we have found reduces the R_nA products by a factor of 3-6 relative to *in-situ* ion mill cleaning [6]. The normal metal is 75 Å of $Co_{0.2}$-YBCO and the counterelectrode is $La_{0.05}$-YBCO, deposited under standard conditions. It is clear from the table that *the La-doped base electrode results in a dramatically higher device resistance and lower J_c compared to the pure YBCO base electrode*, which has an R_nA product within a factor of three of the zero interface resistance limit. We have also observed that the Co-YBCO junction resistances are dependent upon the method of base electrode deposition. For example, sputtered YBCO base electrodes typically exhibit R_nA products roughly 0.3 to 1 times that of PLD $La_{0.05}$-YBCO base electrodes for devices with similar processing conditions.

Co-YBCO edge junctions produced with the sputtered or $La_{0.05}$-YBCO base electrodes typically exhibit RSJ I-V characteristics and have resistances suitable for SFQ digital applications. Fig.1 shows the 55 K I–V curve and its derivative for a ten-junction series array with a sputtered YBCO base electrode and a 50 Å $Co_{0.2}$-YBCO interlayer. Extraction of the minimum and maximum critical currents from the dV/dI curve gives an I_c 1-σ of 6% for this array. On an adjacent individual junction test subchip with 20 devices the average parameters and spreads at 55 K were: $J_c = 1 \times 10^5$ A/cm^2, 1-σ = 10%; I_cR_n = 797 μV, 1-σ = 6%; and R_nA = 0.77 Ω-μm^2, 1-σ = 5%. More generally, the J_c spreads for our high R_nA Co-YBCO junction process are in the 10-30% range. The high resistance junctions also typically show

TABLE I

R_nA AND J_c DEPENDENCE ON BASE ELECTRODE COMPOSITION

Base electrode	R_nA (Ω-μm^2)	J_c(A/cm^2)
PLD La-YBCO	0.82	1.22×10^3
PLD YBCO	0.07	2.1×10^5

Average SNS chip data at 77 K showing dependence of R_nA and J_c on base electrode material. The base electrodes have CeO_2 cap layers and were cleaned using Br etching. The $Co_{0.2}$-YBCO N-layers are 75 Å thick and the counterelectrodes are $La_{0.05}$-YBCO.

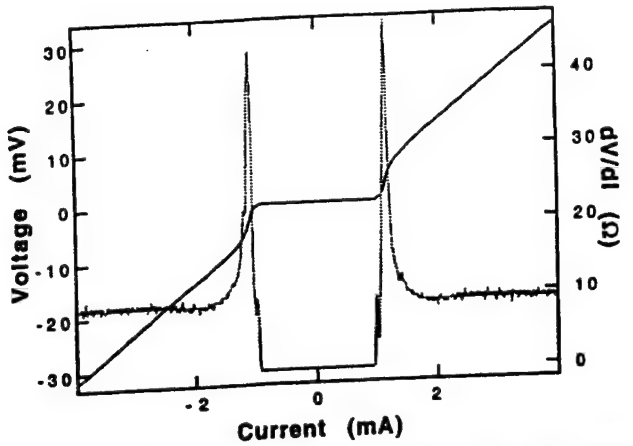

Fig. 1. I-V data at 55 K for a high R_n ten junction series array. Analysis of the dV/dI curve yields an I_c spread of 6%. Individual junction measurements on the same chip give $R_nA = 0.77\ \Omega\text{-}\mu m^2$ and $I_cR_n \approx 800\ \mu V$.

Fraunhofer-like $I_c(B)$ modulation indicating relatively uniform conduction through the normal metal [6]. In addition, proximity-effect fits of the temperature dependent critical current of the high R_n devices give sensible values for the normal metal coherence length.

B. Hot Ion Damage Weak Links

Our principle results for the HID process are summarized in Fig. 2, which shows a plot of junction R_nA vs. ion milling time for three different base electrode types. In this case the ion damage was done using 200 eV Ar ion bombardment at 400°C followed by a vacuum anneal at the same temperature and counterelectrode deposition at 790°C. The data at zero milling time will be discussed in the next section. We see that a large increase in R_nA occurs for the LaYBCO base electrodes between 3 and 6 minutes, while the PLD-YBCO electrodes show a significantly higher threshold, and there is essentially no increase in R_nA for the coevaporated YBCO electrodes. A key point is that the hot ion damage process is able to tune the LaYBCO and PLD-YBCO device resistances into the range useful for digital applications (shown as the shaded region). Furthermore, the I–V curves of the devices in this range are RSJ-like and have practical values of I_c and I_cR_n in a useful temperature range (≈65 K and below) as shown in Fig. 3. At 65 K the average junction parameters for this chip are $J_c = 3.7 \times 10^4$ A/cm^2, 1-σ = 33%; $I_cR_n = 266\ \mu V$, 1-σ = 18%; and $R_nA = 0.76\ \Omega\text{-}\mu m^2$, 1-σ = 16%.

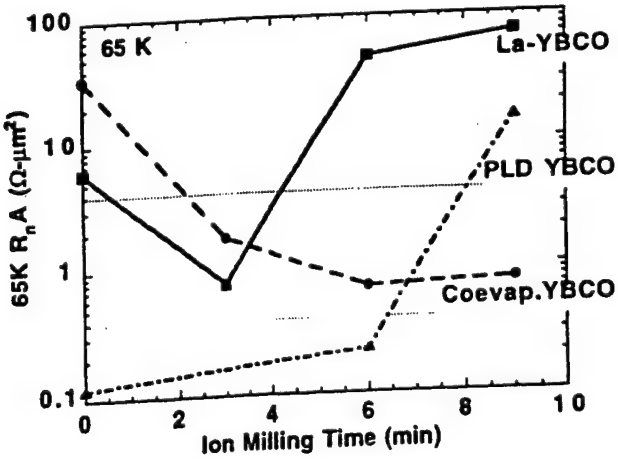

Fig.2. Plot of HID junction R_nA vs. ion milling time for three base electrode types using 200 eV Ar ions at 400°C followed by a vacuum anneal at 400°C and counterelectrode deposition at 790°C.

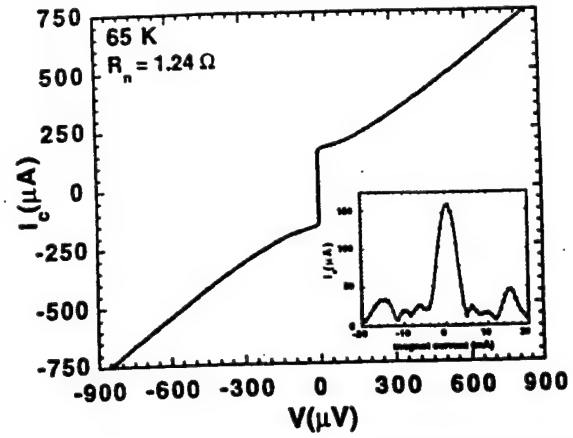

Fig.3. I–V characteristics and $I_c(B)$ modulation at 65 K for an HID junction with a La-YBCO base electrode produced by 200 eV Ar ion damage at 400°C for 3 minutes followed by a vacuum anneal and counterelectrode growth at 790°C.

C. Controlled Interfacial Disorder Junctions

The CID process relies on disorder at the base electrode - counterelectrode interface to form a Josephson junction. We have found that this disorder can be controlled by the base electrode material and the growth conditions of the counterelectrode. The effect of the base electrode composition is shown by the points at zero milling time in Fig. 2 for a process using Br edge cleaning with a 400°C vacuum anneal followed by counterelectrode overgrowth at 790°C. The R_nA products range from 0.12 Ω-μm^2 for the PLD undoped YBCO base electrode to 6.1 Ω-μm^2 for the $La_{0.05}$-YBCO to 34.2 Ω-μm^2 for the coevaporated YBCO material. Interestingly, a light ion treatment has the effect of *reducing* R_nA for the La-YBCO and coevaporated base electrodes, perhaps due to removal of a thin Br-reacted surface layer, or by changing the base electrode surface reconstruction and thus affecting overgrowth of the counterelectrode.

For devices with LaYBCO base electrodes and R_nA in the range of a few Ω-μm^2 initial results show that increasing the counterelectrode growth from 790°C to 805°C reduces R_nA by roughly a factor of two, while vacuum annealing can increase R_nA by up to a factor of five. For the higher resistance coevaporated YBCO base electrodes, increasing the counterelectrode growth to 805°C results in more than an order of magnitude drop in R_nA. By adjusting these conditions, the CID process is able to produce junctions with RSJ I–V characteristics and device resistances compatible with digital applications. Fig. 4 shows the I-V characteristics for a CID junction at 55 K, produced using a Br-etched La-YBCO base electrode with no vacuum anneal and counterelectrode overgrowth at 805°C. In this case the average junction parameters are $J_c = 4.2 \times 10^4$ A/cm^2, 1-σ = 19%; $I_cR_n = 699$ μV, 1-σ = 21%; and $R_nA = 1.69\ \Omega\text{-}\mu m^2$, 1-σ = 17%.

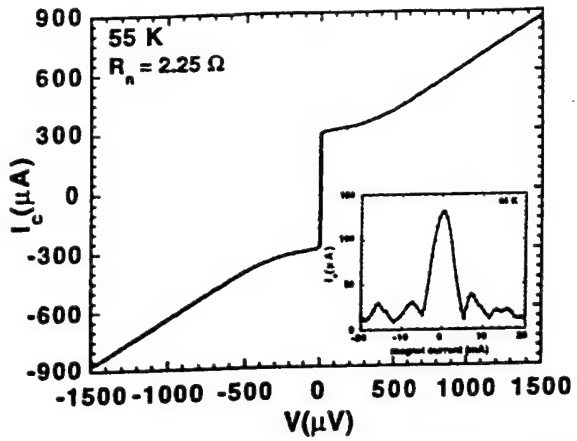

Fig.4. 55 K I–V characteristics and I_c(B) modulation at 65 K for a CID junction with a La-YBCO base electrode completed by counterelectrode growth at 805°C without a vacuum anneal.

IV. Discussion

We have fabricated three different types of HTS edge-geomety weak links using either epitaxial Co-YBCO normal metal interlayers to form SNS junctions; or ion damage or inherent interfacial disorder to produce weak links defined without any deposited interlayer. For all three types of devices we find that base electrode composition and the growth conditions for the epitaxial overlayers have a strong effect on junction resistance. The fact that these variables have a similar influence in each case suggests a common mechanism of interface resistance formation. One strong possibility is that the base-electrode-dependent resistance in these devices is due to cation disorder near the base electrode surface. It is known that cation disorder, such as Y and Ba interchange in YBCO, can lead to suppression of T_c in the HTS materials and that cation disorder is more prevalent in superconductors with cations having similar ionic radii [6]. Indeed we see the largest junction resistances for base electrodes with cations that are relatively close in size such as La-doped YBCO where La may interchange more readily with Y than Ba can. This is consistent with the increased ion damage sensitivity seen for the PLD La-YBCO electrodes relative to PLD YBCO. We also speculate that YBCO base electrodes deposited by various techniques have different amounts of cation disorder leading to the differences in junction resistance seen in these cases. For example, in the case of the coevaporated films grown at low temperatures (≈650°C), there may be enough preexisting cation disorder that the ion treatments have little additional effect, as seen in Fig. 2.

We have also seen that the normal metal (for the SNS case) and counterelectrode growth conditions can play a major role in controlling device resistances. The dependence on growth parameters demonstrates that, in general, the device resistances are not determined entirely by a pre-existing surface layer on the base electrode edge. Both the epitaxial template (i.e. the base electrode surface) and the overlayer growth conditions can affect the initial stages of epitaxy. This suggests that there is also a contribution to the interface resistance from defects in the overlayer microstructure "frozen in" during the early part of overlayer growth.

Overall, the best J_c spreads have been observed for the Co-YBCO SNS junctions. However, on average the SNS devices and the HID and CID weak links without deposited interlayers have comparable parameter spreads with J_c 1-σ generally in the 10-30% range for devices with SFQ-compatible resistances. This suggests that inhomogeneities in the Co-YBCO are not the primary factor limiting progress towards smaller J_c spreads. Rather, we believe that tighter spreads will result from improvements in base electrode morphology and in the growth of the counterelectrodes.

In summary, we have shown that high resistance HTS weak links can be fabricated in a number of ways both with and without deposited interlayers. The resistances are strongly affected by a number of factors, including the the base electrode material, and the deposition parameters of the overlayers. The interface resistance is believed to be associated with cation disorder at the base electrode interface as well as with defects near that interface frozen in during growth of the overlayers. By choosing the proper base electrode material and overlayer growth conditions, it is possible to fabricate high quality edge junctions with a wide range of interface resistances ranging from almost no interface resistance to cases where the interface resistance is dominant. Importantly, even in the high resistance limit required for SFQ applications the SNS junctions still behave like true proximity effect devices. All three types of devices show reasonable I_c(B) modulation and I_c spreads approaching the values needed for SFQ circuits.

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HTS SFQ T-Flip Flop with Directly Coupled Readout

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Abstract--**The authors report the design, fabrication, and test results of single flux quantum (SFQ) toggle flip flop circuits. These circuits, investigated as building blocks of an HTS counting ADC, feature a directly coupled readout junction stack similar to those used in LTS RSFQ circuits. The directly coupled circuit delivers higher readout voltage, hence potentially higher operating speed than magnetically coupled alternatives. The circuits were fabricated using two multilayer HTS SNS junction integrated circuit technologies (one at Northrop Grumman and the other at TRW) featuring three YBCO depositions. Initial testing demonstrated toggling of a T-flip flop in response to SFQ pulses generated by integrated dc/SFQ converters. The readout voltage is shown to approach 40% of the junction I_CR_N product, and as high as 100 μV at 65K. Test results are compared with predicted fabrication process parameter requirements. To increase margins and tolerance to process parameter variations, improvements to the design have been made using JSpice and MALT.**

I. Introduction

There is great interest in HTS A/D converters operating at relatively high temperatures. For example, use of an HTS A/D converter operating at 30-65 Kelvin would have major advantages for scientific IR sensors, such as those used in Earth observation, and IR focal plane arrays, such as those used for astronomy. Other applications range from communications to instrumentation. Progress has been made in HTS flash A/D converter circuits [1] as well as building block circuits for RSFQ implementations [2]. The combination of high performance, ultra-low operating power, and relatively modest fabrication requirements make the RSFQ approach very attractive.

For example, it would be possible to build a useful A/D converter based on a single, minimum complexity HTS integrated circuit, containing only the RSFQ circuits. The biasing network could be off chip, possibly using discrete resistors selected to customize the bias current values for a particular RSFQ chip, analogous to the select in test (SIT) method commonly used in advanced electronics. *This scenario would require no additional integrated circuit fabrication process features beyond what has already been proven.*

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Recently, it has been emphasized that in addition to building a functioning HTS RSFQ circuit, attention must be paid to thermally generated errors in digital operation in order to build a useful high temperature digital circuit [3], [4]. Considerable effort has been spent recently to predict the minimum bit error ratio (BER) of HTS RSFQ circuits operating at high temperatures. In general, the expected BER is a serious problem for an application like digital computing. The required BER of less than 10^{-19} required for computing may not be possible at 65 Kelvin. The A/D converter, however, can accommodate a higher BER with an acceptable degradation in performance. Recent measurements of HTS RSFQ bit error ratios at temperatures as high as 35 Kelvin are encouraging as they relate to the prospects of building useful high temperature A/D converters [4].

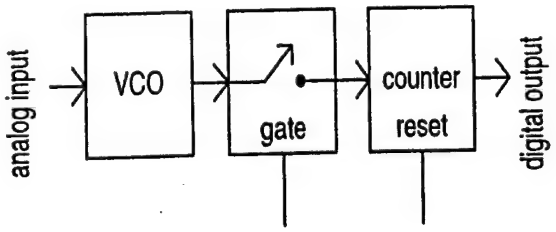

Figure 1. The oscillator-counter ADC. The VCO continuously follows the analog input, emitting pulses at a rate precisely proportional to its voltage. When "gate" is high SFQ pulses are passed from the VCO to the counter, when "gate" is low SFQ pulses are prevented from passing to the counter. The total number of pulses passed in a fixed gate-open time is proportional to the time average of the analog input over the gate-open time.

We have designed, fabricated, and tested HTS RSFQ circuits for use in an oscillator-counter A/D converter, shown in Fig.1. One critical advantage of this architecture for building an HTS A/D converter is the relatively low level of circuit complexity required. A complete 12 bit NbN A/D converter circuit using this architecture required only 52 Josephson junctions. The performance of the A/D converter shown in Fig.1 is determined by the maximum operating frequency of the SFQ circuits. An A/D with 8 bits of SNR at 150 MSPS requires the T-flip flop to operate at 50 GHz.

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impossible using existing two-layer HTS processes. In fact, the process requirements are relatively modest. Two HTS layers with edge junctions in the top layer and superconducting contact between layers is all that is required to build the required RSFQ circuits. HTS edge junctions are well suited for RSFQ circuits. In the longer term, the realistic potential for I_cR_n products above 1 mV may lead to very high speed RSFQ circuits.

Perhaps the most important aspect of the present work is the demonstration of a directly coupled dc readout stack in the usual SFQ-to-dc converter configuration. The readout voltage was as high as 100 μV, and consistently approximately one half of the junctions I_cR_n product. Avoiding magnetically couple readout circuits simplifies fabrication and maximizes output voltage.

II. Design

The SFQ counter shown in Fig.1 consists of a series of SFQ toggle or "T" flip flops. Developing a T flip flop is the first step in building the ADC. Fig.2 is a schematic of the tested SFQ T- flip flop circuit. The circuit consists of a dc/sfq converter, a four-stage JTL, and a T flip-flop with a directly coupled readout (sfq/dc converter). The input signal generates a magnetic flux through the main inductor of the dc/sfq front end. For a rising signal, an SFQ pulse is generated at the output of the dc/sfq every time the flux generated reaches an integer number of flux quanta. The SFQ pulse is then passed along the JTL to toggle the T flip-flop between the 0 and 1 states, corresponding to different directions of its circulating current. The state of the T flip-flop is probed by the direct-coupled readout. In particular, there will be a finite voltage readout when the T flip-flop is in the 1 state. Note that no SFQ pulse is generated at the output of the dc/sfq when the input signal is ramped down.

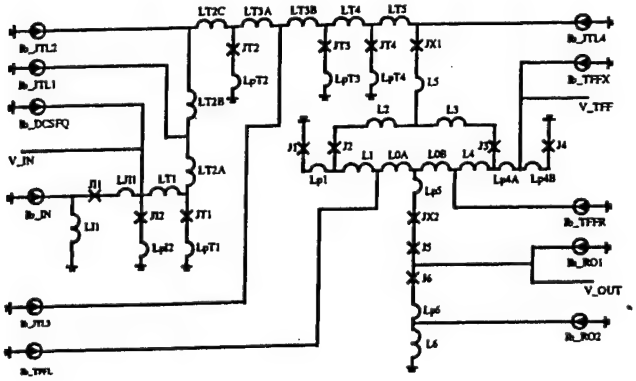

Figure 2. Circuit diagram of the T flip flop with DC/SFQ and SFQ/DC converter. Junctions JI1 and JI2 form a DC/SFQ converter, junctions JT1, JT2, JT3, and JT4 form a JTL, junctions J1, J2, J3, and J4 form a four-junction bridge of the T flip flop, while junctions J5, J6 form the directly coupled sense SQUID. Junctions JX1, JX2 are large Josephson junctions necessary for layer-to-layer connection.
Extracted circuit parameters:

JI1=JI2=JT1=JT2=J2=J3=J5=J6=4μm, JT3=J1=J4=6μm, JT4=8μm, JX1=22 mm, JX2=14 mm,
LI1=2.0pH, LT1=4.8pH, LT2A=0.9pH, LT2B=3.8pH, LT2C=0.5pH, LT3A=2.5pH, LT3B=1.6pH, LT4=3.4pH, LT5=1.4pH, L0A=2.9pH, L0B=2.6pH, L1=L4=1.5pH, L2=L3=4.4pH, L5=1.8pH, L6=1.0pH, LpI1=4.3pH, LpI2=3.5pH, Lp1=3.4pH, Lp4A=1.3pH, Lp4B=1.9pH, Lp5=3.1pH, Lp6=2.4pH

III. Fabrication

The devices were fabricated using an epitaxial multilayer process which integrated edge SNS junctions, using a normal layer of $YBa_2Cu_{2.79}Co_{0.21}O_{7-\delta}$, with a buried YBCO groundplane, in four separate epitaxial depositions. The essential parts of this process have been described elsewhere [5], [6], and here we only outline the process, which uses a combination of pulsed laser deposition (PLD) and off-axis rf magnetron sputtering.

A micrograph of the actual circuit is shown in Fig.3. All layers were patterned using 300V ion milling with 0 to 10% oxygen in argon, at 45° angle of incidence, using a mask of AZ1518 photoresist reflowed at 130°C. This process was designed to produce an edge taper of 20-30° from the horizontal, independent of edge orientation. Immediately before each epitaxial deposition the samples were cleaned, ex-situ, with a combination of rf oxygen plasma, and argon/oxygen ion milling.

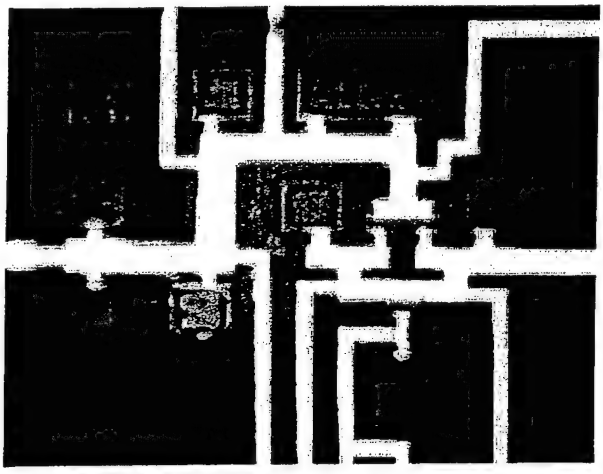

Figure 3. Micrograph of the directly coupled T flip flop test circuit.

Fabrication began with sputter depostion of a 2250Å YBCO groundplane, on a (110) $NdGaO_3$ substrate, typically at 720°C.

After the groundplane was patterned, a 2400 Å $SrTiO_3$ (STO) layer was sputter-deposited at about 680°C, and via holes to the groundplane were etched through the STO. Next, a 2000Å YBCO base electrode and 1500 Å STO capping layer were grown by PLD, at 805°C and 600°C respectively, and patterned. After an *in-situ* Ar ion mill clean we deposited, by PLD, approximately 150 Å of epitaxial Co-doped YBCO, followed by growth of the YBCO counterelectrode, an *in-situ* anneal, and finally *in-situ* sputtering of a gold contact layer near room temperature. Finally the YBCO counterelectrodes were defined with a straight-wall resist process and Ar ion milling. In addition to product chips, each wafer included PCM (process control module) chips to access wafer quality.

IV. Testing

After each wafer was diced, the PCM chips from various dies on the wafer were measured using an automated test station. The result of these measurements addressed the quality and yield of various circuit elements such as strip lines, vias, and junctions. The PCM chips also contained dc SQUIDs similar in structure to those used in the digital circuits. The PCM SQUIDs varied in size. The voltage modulation upon direct injection of a control current was recorded, and the value of inductance per square was extracted. These data, together with visual inspection, offered a reliable way to select digital circuit chips from specific locations on each wafer.

The digital circuit testing was carried out inside a shielded room. The probe used was a TRW made low speed test probe with filtered lines. The probe was inserted into a He flow cryostat with double μ-metal shield. Temperature was regulated by a flow control unit along with a LakeShore 330 temperature controller. This setup allowed us to stabilize the temperature to within 0.02 K. Most of our measurements were carried out at 65 K, the targeted operating temperature. The various dc circuit biases were provided by individual battery powered current sources. This configuration allowed independent adjustments of each bias lines which would accommodate for a larger junction critical current spread. The input signal was provided by a HP 8012B pulse generator with externally connected attenuators. Both input and output signals were directed to a Tektronix 2465B Oscilloscope, with the output signals amplified by PAR113 Preamplifiers.

The counting operation of the circuit, T flip-flop with dc/sfq and sfq/dc converter, was demonstrated at low speed. The test result is shown in Fig.4. The amplitude of the input signal was larger in Fig.4(b) than that in Fig.4(a) so that two SFQ pulses were generated during each rising edge of the ramp, and as a result, the T flip-flop changed state twice. The levels of various bias lines are listed in Table 1, along with the numbers used in JSPICE simulation. The disagreements are likely to have resulted both from the spread of the junction critical current and trapped flux. The latter is supported by the fact that we sometimes obtained different bias levels for correct operation during different cool-downs.

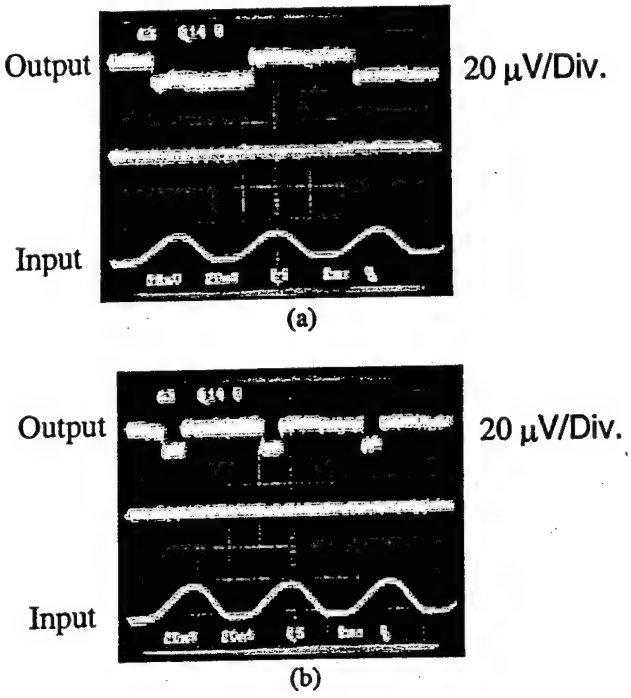

Figure 4. Oscilloscope pictures demonstrating the correct operation of the HTS T flip-flop circuit at 65 K. The center traces shows that the flip flop SQUID voltage stays zero at all times. The T flip-flop toggles when the input signal to the dc/sfq converter reached the threshold values while being ramped up.

TABLE I

Measured bias levels of the T flip-flop circuit, compared to the values derived from simulation.

	Simulation (μA)	Testing (μA)
Ib_{dcsfq}	120	12
Ib_{JTL1}	120	120
Ib_{JTL2}	120	240
Ib_{JTL3}	180	149
Ib_{JTL4}	450	265
Ib_{TFF-L}	230	683
Ib_{TFF-R}	-200	-461
Ib_{RO1}	250	242
Ib_{RO2}	900	830
Input Level per SFQ	1000	490

The above tested circuit had an estimated lowest error rate of 10%, so it was not possible to define the operating bias

margins. We have performed margin and yield analysis with the MALT tool. The simulation results showed that some circuit elements allowed less than 10% in parameter margin, lower than the spread that is achievable by the present fab process. However, MALT simulation also indicated that circuit yield could be greatly increased with improved designs.

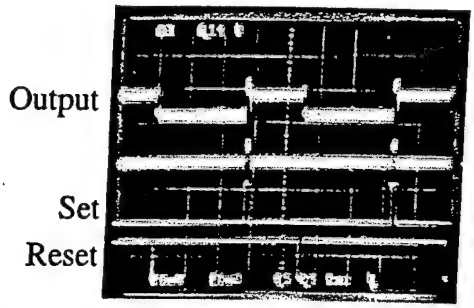

Figure 5. Readout level measured with direct set/reset of the same T flip-flop circuit measured in Fig.4.

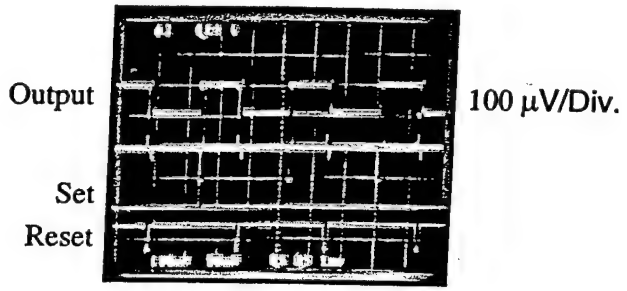

Figure 6. Higher readout level demonstrated with improved junction process.

Many of the circuits fabricated did not function correctly as SFQ circuits, however, it is often still possible to test the direct-coupled readout component. Instead of toggling the T flip-flop with SFQ pulses generated at the dc/sfq and passed through the JTL, we can inject non-SFQ pulses of positive and negative sign into storage SQUID loop of the T flip-flop. This forcefully establishes the direction of the circulation current in the T flip-flop and sets it up in either the 1 or the 0 state. The result of this non SFQ test performed on the fully functional circuit (as shown in Fig.4) is shown in Fig.5. The readout bias Ib_{ROI} is at the same level as that in the SFQ test, shown in Table1. Note that the output is also at the same level as that shown in Fig.4. In this case, the readout voltage and SFQ operation are independent.

The output level is an important characteristic of the circuit. When operating at high speed, the output must exceed a certain voltage level in order to be read by the test electronics. With improved junction characteristics, especially the increase of I_cR_n product and less artificial rounding of the I-V curve shape, we have been able to reach output levels as high as 100 μV with this type of direct-coupled readout, as shown in Fig.6. The average junction I_cR_n product was about 260 μV, indicating that the read out voltage is approaching 40% of the I_cR_n value.

I. Summary

In summary, we have designed, fabricated, and demonstrated the operation of an HTS T flip-flop circuit, including its front end (dc/sfq) and readout (sfq/dc). The readout, in particular, adopted the direct coupled configuration similar to some LTS designs. The readout was shown to be close to 100 μV, approaching 40% of the junction I_cR_n product. Higher output voltage is possible with improving process and design, leading to potentially higher operating speed. This HTS T flip-flop circuit serves as a building block of an HTS ADC.

II. Acknowledgement

The authors would like to thank Ken Daly of TRW Inc. for various discussions during this work and critical comments of the paper.

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HTS JUNCTION AND MULTILAYER INTEGRATED CIRCUIT TECHNOLOGY FOR SFQ APPLICATIONS

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ABSTRACT

We have developed processes for fabrication of high-R_n HTS Josephson junctions using Co-doped-YBCO and Ga-doped-PBCO interlayers, as well as devices with no deposited interlayers. Adjusting the base electrode composition and the growth conditions of the overlayers enables the fabrication of SFQ-compatible junctions with 1-σ J_c spreads of 10-30%. The HTS junctions have been integrated with YBCO groundplanes in multilayer circuit structures with six epitaxial layers. Successful fabrication of multilayer circuits requires careful control of film growth, patterning, surface cleaning, and oxidation. We have used this technology to demonstrate small-scale HTS SFQ circuits, including the first realization of an HTS sigma-delta modulator.

INTRODUCTION

High Temperature Superconductor (HTS) digital circuits based on Single Flux Quantum (SFQ) logic require the fabrication of high quality Josephson junctions integrated with superconducting groundplanes for control of inductances. More specifically, critical current spreads of better than approximately 10% are needed to produce SFQ circuits with several hundred junctions at acceptable yields [1]. Operation at tens of GHz requires I_cR_n products greater than about 300 μV, which points to device resistances on the order of an ohm at typical SFQ operating currents. Significant efforts have been directed at the fabrication of HTS junctions with deposited epitaxial interlayers such as Co-doped YBCO [2,3] and Ga-doped PBCO [4]. Previous success at achieving narrow J_c spreads with "artificial barriers" in low-T_c materials indicates that *there is no fundamental problem with deposited interlayers* [5]. However, processes without deposited interlayers have also produced high quality weak links [6,7,8] and are worth investigating as another means of fabricating SFQ-compatible junctions. In this paper we describe our device results for both types of approaches, which we find give comparable baseline junction parameter spreads. We also summarize the processes we use to integrate HTS junctions in functional multilayer circuits containing up to nearly 40 devices, and discuss the initial results for an HTS sigma-delta modulator.

HTS JUNCTION FABRICATION DETAILS

Much of our junction fabrication effort has focused on optimization of superconductor / normal-metal / superconductor (SNS) weak links utilizing $YBa_2Cu_{2.8}Co_{0.2}O_{7-\delta}$ as the normal metal interlayer. The basic details of our edge junction process have been presented previously [3,9,10,11,12], but an overview of the fabrication with new details will be given here. At present, HTS film growth is done using pulsed laser deposition of $YBa_2Cu_3O_{7-\delta}$ (YBCO) or $YBa_{2-x}La_xCu_3O_{7-\delta}$ (La-doped YBCO). The target-to-substrate distance is 5 cm and the laser spot (4.9 mm^2) is scanned along a target diameter with a 1-2 cm diameter gap in the center of the scan range to improve uniformity. YBCO growth temperatures range from a nominal 805• C to 820• C in a 300 mT oxygen atmosphere. The base electrode edges are patterned using reflowed photoresist and 150 eV Ar ion milling at 45• with rotation, and then are typically cleaned using a sequence of an oxygen plasma, Ar/O_2 milling, and Br etching. Following edge cleaning and silver paint mounting on a substrate block in a dry box, the Co-YBCO and counterelectrode are grown and patterned.

More recently we have extended this process to fabrication of "SNS" weak links using $PrBa_2Cu_{2.9}Ga_{0.1}O_{7-\delta}$ as the interlayer. Test runs modeling growth of the interlayer and counterelectrode indicated that YBCO grown over a 50Å Ga-PBCO layer was primarily a-axis oriented with a high resistivity and depressed T_c. However, we found that these problems could be minimized by growing at higher temperatures (820• C, limited by our heater) and by including a 50Å pure YBCO buffer layer below the Ga-PBCO film to aid in proper nucleation of c-axis growth. Such a YBCO/Ga-PBCO bi-

layer forms the interlayer in our present Ga-PBCO junction process. Otherwise the process is essentially identical to Co-YBCO junction fabrication.

We have also developed an alternate junction process which utilizes ion damage at elevated temperatures to form HTS Josephson junctions without a deposited interlayer [12]. This "hot-ion-damage" (HID) process starts with the same *ex-situ* cleaning procedure used for our SNS junctions. The cleaning is followed by an *in-situ* Ar or Xe ion mill treatment at 400• C at a beam energy of 100 - 300 eV with a total beam current of 5 mA in our 3 cm mill. Typical treatment times are 3-15 minutes. After the mill process, a vacuum anneal is done for 30 minutes at 400• C, the heater is ramped up to 790-805• C in oxygen, the counterelectrode is deposited, and the chips are then annealed as usual at 450-500• C in 500 T O_2.

HTS JUNCTION RESULTS

Our results for SNS junctions using Co-doped YBCO as the normal metal have been described in previous publications [3,9-12]. One principal finding has been that the device resistances are strongly affected by the base electrode composition and the growth conditions for the normal metal and counterelectrode. In particular, we have discovered that $YBa_{1.95}La_{0.05}Cu_3O_{7-\delta}$ base electrodes produce SNS device resistances approximately an order of magnitude higher than devices using PLD-deposited YBCO base electrodes. This is an important result because devices incorporating base electrodes of La-doped YBCO rather than undoped YBCO have much higher effective I_cR_n products at typical SFQ operating currents. The best J_c spreads we have observed in junctions with SFQ-compatible critical currents and resistances are 6% in 10-junction series arrays and 11% in 100 junction series arrays. While these are very encouraging results, more typically we see 1-σ J_c spreads in the 10-30% range. Consequently we have been motivated to examine other junction technologies including Ga-doped PBCO. Figure 1 shows our initial results for junctions with a 50Å Ga-doped PBCO interlayer fabricated using the process described above. The key features to note are that the I_c and R_n of this device are in the range needed for SFQ applications and that the 920 μV I_cR_n product is among the highest reported values at this temperature. The inset shows close-to-ideal critical current modulation, indicating good uniformity even for a 50Å interlayer. Finally, the 1-σ J_c spread for this chip was 19%, which is a promising initial result.

For junctions without deposited interlayers we have focused on both HID junctions as well as a process which uses controlled interfacial disorder (CID) to form Josephson junctions without an ion treatment [12], but the CID results will not be discussed here. The hot ion damage weak links exhibit RSJ-like I-V characteristics with reasonable $I_c(B)$ modulation. Similarly to the Co-YBCO devices, the HID junctions show significantly higher resistances for La-doped YBCO versus pure YBCO base electrodes for all ion doses we have investigated. For a 200 eV Ar ion treatment at 400• C with La-doped base electrodes, devices have an average resistance of 0.93 • with average I_cR_n products of approximately 600 μV and a 1-σ J_c spread of 29%.

For devices with or without a deposited interlayer, we find that base electrode composition and the growth conditions for the epitaxial overlayers have a strong effect on junction resistance. . We believe that the base-electrode-dependent resistance is due to cation disorder near the base electrode surface [11]. Overall, the best J_c spreads have been observed for the Co-YBCO SNS junctions. However, on average *every junction approach we have investigated gives comparable parameter spreads* with J_c 1-σ generally in the 10-30% range for devices with SFQ-compatible resistances. This suggests that inhomogeneities in the deposited interlayers are <u>not</u> the primary factor limiting

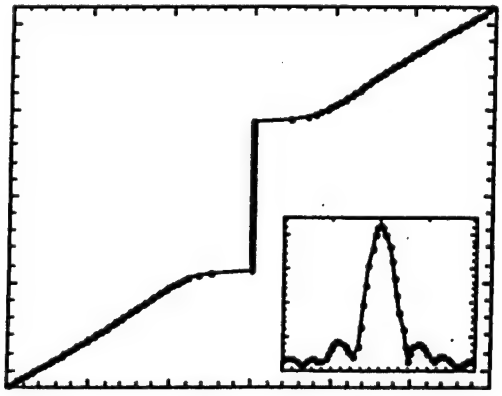

Fig. 1 I-V characteristics and $I_c(B)$ (inset) for a device with a 50 Å Ga-doped PBCO interlayer.

progress towards smaller J_c spreads. Rather, we believe that tighter spreads will result from improvements in base electrode morphology, in the edge formation process, and in growth of the device overlayers.

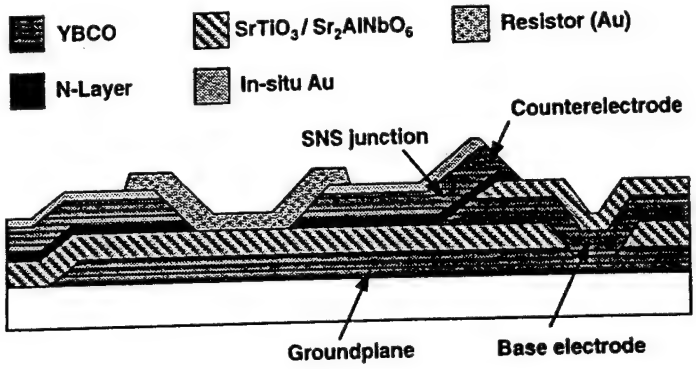

Fig. 2 Cross-sectional schematic of multilayer HTS circuit with six epitaxial layers.

CIRCUIT FABRICATION

To produce practical SFQ circuits high quality HTS junctions must be integrated with a superconducting groundplane, and generally with resistors as well. Figure 2 shows a cross-sectional schematic of our typical circuit configuration which uses a buried YBCO groundplane, although we have also fabricated junctions with groundplanes on top [10]. There are six epitaxial layers in the structure of Fig. 2, grown in four separate depositions with film patterning in between [3,9,10]. We have also developed a more complex process, which utilizes an additional patterned epitaxial insulator over the device edges to enable fabrication of low inductance "slot-defined" junctions and gives more wiring flexibility [9,13].

Requirements for successful fabrication of this type of circuit include the need for acceptable electrical isolation, high J_c vias and crossovers, high quality epitaxy of all layers, SFQ-compatible junctions, and complete oxidation of buried YBCO films. In practice, meeting most of these constraints requires the production of smooth, outgrowth-free films. Of course an essential condition for producing smooth films is a well-optimized film deposition process. But, beyond that, maintaining high quality epitaxy in a multilayer structure is critically dependent on surface cleaning of processed films before growth of the next epitaxial layer. We have developed a cleaning process which gives acceptable yields for smooth film growth. This process uses an oxygen RIE plasma treatment followed by an *ex-situ* 2-3 minute Ar/O_2 ion mill (20% O_2) at 150 eV. In cases where a significant amount of exposed YBCO is present we also do a 10-30 sec Br in methanol etch (0.3%). In addition, we have found that an *in-situ* Ar ion mill cleaning before growth of the base electrode bilayer improves the base electrode J_c.

Functional circuit crossovers and vias must transport at least several mA of current without entering the voltage state. Previous work had shown us the importance of film edge angles in determining junction properties and film morphology [9]. Consequently we examined the effect of edge angle on groundplane crossovers and on vias. Surprisingly, we found that shallow (• 15•) groundplane edge angles produced acceptably high J_c crossovers, while steeper via edge angles (• 30•) were needed to obtain useful via current densities. Crossover and via J_c values as well as groundplane shielding properties are strongly dependent on oxidation of the buried YBCO films. Oxygen transport through the base electrode and groundplane insulator layers is a strong function of the epitaxial quality of the insulator layers. In particular it is useful to grow the insulator layers (usually $SrTiO_3$, "STO") at temperatures below the temperature which gives optimum epitaxial quality [3]. For our PLD process, STO growth at 750• C usually gives reasonable oxygen transport properties. Oxygen transport can also be increased by annealing at 520• C. Although that temperature does not allow the optimum equilibrium oxygen content in YBCO, it generally gives T_c values above • 85K for two hour annealing times, which is acceptable for our circuit applications. In the less common cases where oxidation of the buried YBCO is very slow, a plasma oxidation process can be useful [14].

Of course a key issue is obtaining high quality junctions over the buried groundplane. In fact, we find that junctions over groundplanes are usually (but not always) comparable to adjacent junctions without groundplanes. Figure 3 gives the I-V characteristics at 45K for some recent Co-YBCO test junctions over groundplanes on the same chip as a set of 4-bit counting A/D circuits. The average critical current is 503 μA and the average resistance is 0.95 • . The 1-σ J_c spread for these SFQ-compatible junctions was 14% while the R_nA and I_cR_n spreads were 7%. $I_c(B)$ and SQUID studies on junctions over groundplanes have demonstrated the functionality of the buried groundplanes and indicate a microstrip inductance of about 1 pH/sq. at 65K [3,13].

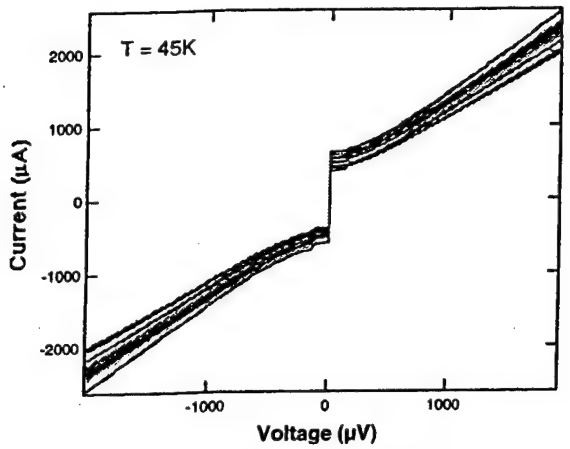

Fig. 3 I-V characteristics for junctions over a groundplane with a 100Å Co-YBCO normal metal layer.

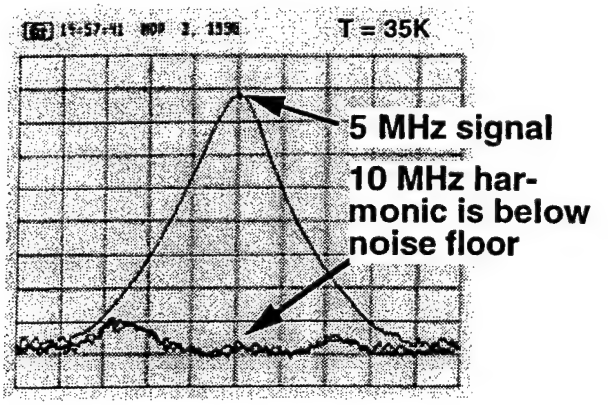

Fig. 4 Spectrum analyzer output for HTS modulator with 5 MHz input. The 10 MHz harmonic is below the noise floor, giving a SFDR better than 75 dB.

HTS SFQ CIRCUIT DEMONSTRATIONS

We have used the multilayer fabrication technology described above to demonstrate a number of small scale SFQ circuits [15]. Most recently we have worked on a four-bit counting A/D converter and an HTS sigma-delta modulator [16]. The four-bit A/D with 39 junctions showed correct operation of each individual bit, but multibit operation was not achieved, possibly due to the lack of buffers between each T flip-flop stage. The sigma-delta modulator forms the basis for a high dynamic range A/D converter. This device oversamples an input signal and converts it to a digital bit stream which is then digitally filtered to provide a high dynamic range output. Using SFQ logic allows oversampling at tens of GHz clock rates. This sampling rate enables implementation of an 18-20 bit A/D at 10-20 MHz, which is important for radar and other applications. As an initial demonstration of this approach, we have fabricated a simple HTS sigma-delta modulator containing 14 junctions with a buried YBCO groundplane and Au bias line resistors. We have measured the modulator performance using a 5 MHz input signal. The modulator output bit stream was sent into a spectrum analyzer to meaure the relative amplitude of the unwanted harmonics which determine the spur-free dynamic range (SFDR). As shown in Figure 4, with a 27 GHz sampling rate we measured a SFDR > 75 dB, comparable to our previous test of an LTS modulator. Two-tone tests showed third-order intermodulation products to be less than -57 dBc.

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HTS MULTILAYER PROCESS DEVELOPMENT FOR DIGITAL CIRCUITS

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Abstract

Digital circuits based on High Temperature Superconductors (HTS) have the potential for offering operation at higher speed, and lower power dissipation than semiconductor circuits, while offering unprecedented performance advantages attributable to the unique quantum mechanical nature of the superconducting state. In order to fully realize this potential, it is necessary to develop a circuit process which integrates reproducible Josephson junctions into epitaxial multilayers. This paper discusses some of the materials and fabrication issues involved in the development of such a process.

1. Introduction

Superconducting digital circuits based on Single Flux Quantum (SFQ) logic hold the promise of operating at clock frequencies in the tens of GHz, while dissipating only microwatts per gate. SFQ logic is particularly well suited to moderate size circuits which perform various specialized digital signal processing functions, in applications such as infrared focal plane image processing, encrypted communications, and radar.

The future of HTS digital is shown by the path that LTS digital is following today. One area of intense activity in LTS is high speed analog to digital converters (ADCs), backed by fast digital filters, for sensor applications that require large dynamic range [1–4]. Digital filters, whose

fundamental building block, the multiply-accumulator, was recently demonstrated in LTS [5], are also being applied to enhance the accuracy of GHz-bandwidth ADCs [6].

Josephson digital logic is potentially useful in high-speed data switching for "information highways" [7,8], and for spread spectrum communications, where it offers low-power, high-speed code generators [9,10]. In fact, Josephson digital circuits are so fast that standard semiconductor test equipment can not follow their logic operations, so that on-chip buffers are being used to supply test vectors and capture outputs at GHz rates [11].

As HTS Josephson junctions become more reproducible the high speed of SFQ circuits will become attainable in the more easily utilized 65–77 K temperature range, albeit with somewhat higher power dissipation than in LTS circuits. This allows for the possibility of HTS digital circuits being used in a wide variety of applications where the weight and power requirements of a 4.2 K cryocooler are unacceptable.

2. Process Requirements

Realizing the potential of SFQ circuits in HTS will require the development of an integrated circuit process for these complex, multi-element, anisotropic materials. The requirements on this process include:

- Superconducting films with high critical current density ($> 10^6$ A/cm^2 at 77K), low penetration depth (< 0.25 μm at 65 K), low RF losses ($R_s < 0.5$ mΩ at 10 GHz and 77 K), smooth morphology (RMS roughness < 2 nm), a high degree of crystalline perfection, and stability with respect to such factors as time, thermal cycling, environmental effects such as moisture, and packaging processes;
- Reproducible Josephson junctions, with high characteristic voltages, $V_c \equiv I_c R_N$ (> 300 μV at 65 K), where I_c and R_N are the junction critical current and resistance, respectively;
- Epitaxial insulators which are structurally and chemically compatible with the superconductor layers, with low to moderate dielectric constant ($\varepsilon < 25$), low RF losses, low pin-hole density, and smooth morphology;
- Superconductor-to-superconductor contacts, and superconductor-insulator-superconductor crossovers, with high critical current density and low inductance;

- Possibly epitaxial resistor materials compatible with the superconductor and insulator films; and
- Low-resistance, high-adhesion contacts with metals such as gold.

Certainly the key element of the circuit process is the Josephson junction, and the most important property to which the process development must be directed is *reproducibility, and uniformity of critical current.* This is the main factor in determining the yield of working circuits. Given certain design margins for a circuit (that is, ranges of an operating parameter, such as a bias current, within which the circuit will operate correctly), the junction critical currents must not deviate from this range. For well-designed SFQ circuits it is reasonable to expect margins of ± 30%. Assuming a Gaussian distribution of critical currents, with a certain standard

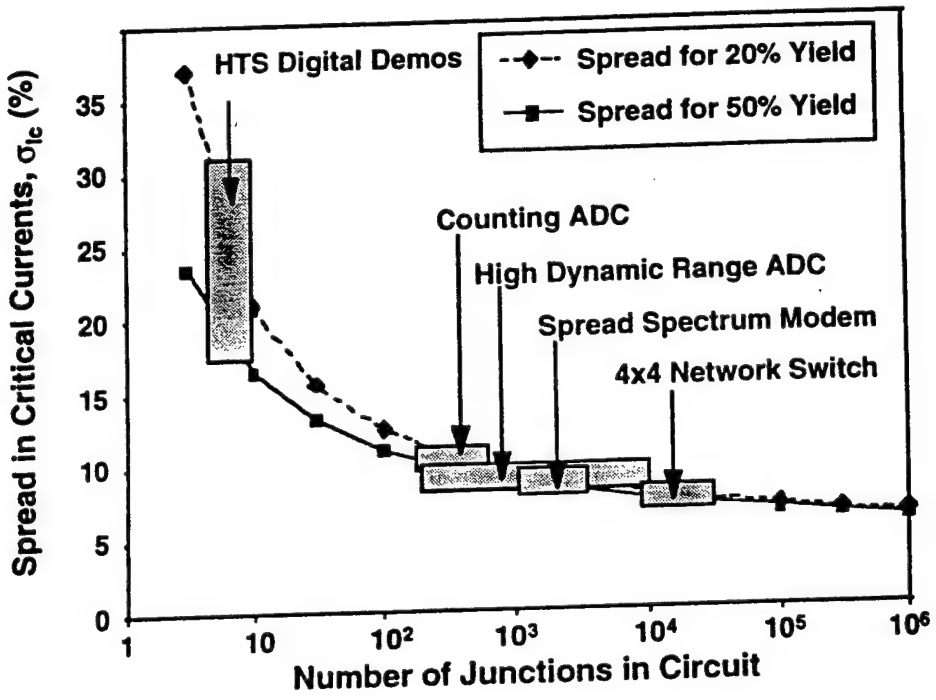

Figure 1. The spread in junction critical currents, σ_{Ic}, required to produce circuits with a given number of junctions. HTS digital circuits demonstrated to date have contained up to about ten junctions, consistent with the typical obtained spreads of 15 to 30%. Useful circuits, requiring 100 to 1000 junctions, will require spreads of about 10% or less.

deviation, σ, one can calculate the expected yield for circuits with a given number of junctions [12]. Figure 1 shows the result of such a calculation, and shows the critical current standard deviation required to obtain yields of 20% and 50%, for circuits of a given junction count. So, for example, to obtain a 50% yield of circuits with 1000 junctions one must have a one-sigma critical current spread of about 9%. Figure 1 illustrates that as spreads are reduced to the 10% range, the achievable circuit complexity increases dramatically for small gains in reproducibility. Of course those small gains may well become increasingly difficult to achieve.

Figure 1 also shows approximate ranges of junction count for various representative circuits for which superconductivity offers potential advantages over competing technologies. A review of these applications is beyond the scope of this article. Demonstrations of HTS digital circuits to date, some of which are described in Section 5.6, have so far been limited to roughly ten junctions or less, which is consistent with the fact that typical I_c spreads are in the 15 to 30% range.

In addition to having reproducible junctions, it is important that inductances be kept low, which is most practically achieved by integrating the Josephson junctions with a high-quality superconducting groundplane. In SFQ circuits the product of critical current, I_c, and inductance, L, is constrained to be of order the flux quantum, $\Phi_o = 2.07 \times 10^{-15}$ Wb. This is particularly difficult for HTS since stability against thermal noise dictates that the critical current should be as large as possible, while still meeting this constraint. In addition, the relatively long magnetic penetration depth in HTS (λ_o = 150 nm for YBCO, compared to 39 nm for Nb) makes inductances higher for given superconducting layer thicknesses.

Estimates of bit-error-rates for HTS circuits are an area of some controversy, but it is likely that many applications which require extremely low error rates (say 10^{-20} sec^{-1}) will never be practical in HTS. However, some applications of interest, such as ADCs, may tolerate much high error rates (~ 10^{-9} – 10^{-6}), and thus should be practical in HTS. Even to maintain these error rates it is likely that junction critical currents will need to be about 0.5 mA, so that a constraint of $LI_c = \Phi_o$ leads to an inductance of about 4 pH. As we sill see later, this is a significant challenge, and will require a complex multilayer process, and a good deal of ingenuity.

In this article we discuss some of the materials and processing issues involved in the development of such a process. The discussion will use as a basis our own experience in demonstrating two prototype processes which meet many, though not all, of the above requirements.

3. Epitaxial Film Deposition

3.1. YBCO FILMS

YBCO is currently the material of choice for HTS multilayer circuit development because high-quality films can be grown *in situ* by a wide variety of deposition methods, and can be optimized to have very smooth surface morphology (RMS roughness < 1 nm). The three most important deposition techniques for YBCO, as well as for related epitaxial insulators, are sputtering, pulsed laser deposition (PLD), and co-evaporation.

A detailed review of these deposition techniques is beyond the scope of this article. Recent reviews of this area can be found in the references [13,14,15]. Here we mention only a few aspects of importance to multilayer circuit development.

We routinely use off-axis rf magnetron sputtering from a single, press-and-sintered, nominally stoichiometric target to produce films on two-inch wafers, or on several 1-cm square substrates. By adjusting sputtering conditions, such as argon and oxygen pressures, temperature, and geometry, it is possible to produce YBCO films with excellent superconducting properties – $T_c > 90$ K, $J_c > 10^6$ A/cm^2 at above 80 K, and rf surface resistance as low as 0.2 mΩ at 10GHz and 77 K. Such films however often suffer from a high density (~ 10^6 cm^{-2}) of second-phase outgrowths, or "boulders", which are unacceptable for multilayer devices. In practice we adjust the deposition conditions to obtain a surface with as low a density of such outgrowths as possible (10^2 cm^{-2} is acceptable), which typically compromises the superconducting properties somewhat. For example, T_c's of 85–87 K are typical, with J_c still exceeding 10^6 A/cm^2 at 77 K. This necessity for compromise is not unique to sputtering, but is also typical in co-evaporated films [16]. Such films may exhibit RMS roughness as low as 1.0 nm, comparable to the smoothest films obtained by any technique.

Negative aspects of off-axis sputtering, in our experience, include slow deposition rate (typically 10 to 40 nm per hour), and relatively poor run-to-run reproducibility. The latter may be associated with changes in the sputtering target as a function of time, such as the erosion of the "racetrack" groove typical in magnetron sputtering, or compositional or density inhomogeneities in the target material. The presence of the spatially extended plasma may also cause preferential resputtering of

material from the deposition chamber hardware, leading to additional copper, for example, being present at the substrate [17].

Pulsed laser deposition offers much higher deposition rate, typically of order 1.0 Å/second, but potentially orders of magnitude higher [15]. The technique is also extremely flexible in that a wide range of materials can be deposited in a given chamber using multi-target carousels now widely available. Since the laser-target interaction is confined to a relatively small volume there is much less potential for the incorporation of contaminants from the chamber hardware than in the case of sputtering. Although PLD is most easily applied to deposition over relatively small areas (~25 mm diameter), various approaches to rastering the beam, target, and substrate can be used to coat diameters as large as 125 mm [18].

The main disadvantage of PLD is the presence on the film of micron-sized particles which have been ejected from the target. This problem can however be greatly reduced by use of off-axis PLD, where the substrate is placed parallel to the axis of the plume of material emerging from the target [19]. Just as for sputtering it is necessary to carefully optimize deposition parameters, such as pressure, temperature, laser energy density and repetition rate, and target surface preparation, in order to avoid the formation of second-phase outgrowths in the YBCO films.

Some of the first HTS films were deposited by coevaporation from elemental sources, either electron beam or thermal [20]. Some of the difficulties encountered in applying this technique to *in situ* growth were associated with the fact that the film requires a zone of high oxygen pressure to oxidize the material, while the evaporation sources need to be in a low pressure in order to ensure ballistic transport of the metal atoms. While the use of a relatively low pressure of atomic oxygen or ozone was successful in producing high-quality films, the coevaporation technique has recently come into its own with the invention of a heater scheme which has the substrates on a rapidly rotating platen which alternately exposes the substrate to an enclosed oven at 2 Pa pressure of oxygen, and an opening through which the evaporants arrive at the substrate from a much lower pressure region (0.01 Pa). This technique has already been used to coat substrates as large as 8 inches in diameter, or twelve 2-inch substrates at a time. This large area capability, combined with deposition rates of 20 nm/min, make the process extremely efficient [21,22].

3.2. EPITAXIAL INSULATOR FILMS

The same deposition techniques used for HTS films are routinely used to deposit various epitaxial insulators in the fabrication of multilayer devices. Table 1 lists some of the materials routinely used with YBCO, along with their crystal structure, and bulk values of the lattice constant, dielectric constant, and loss tangent. The most developed material is $SrTiO_3$, but its high values of dielectric constant and loss tangent make it undesirable for high frequency applications. While CeO_2 and ZrO_2 are widely used, especially as buffer layers, we favor materials cubic perovskite materials which are lattice matched to YBCO, and which have relatively low dielectric constants, such as Sr_2AlTaO_6 or Sr_2AlNbO_6.

A common problem with epitaxial insulator growth over YBCO is that the rate of oxygen diffusion through the insulator is so low that it is practically impossible to oxygenate the underlying YBCO [23]. In practice one can reduce the insulator deposition temperature enough so that the resulting increased defect density allows oxygen diffusion, though not so low

TABLE 1. List of epitaxial insulators compatible with YBCO, and some of their material parameters. Many of these are also used as substrates. In cases where YBCO grows rotated with respect to the insulator the relevant diagonal distance, or simple fraction thereof, is listed for comparison with YBCO.

Material	Structure	Bulk Lattice Constant (Å)	Bulk Dielectric Constant	Bulk Loss Tangent
$LaAlO_3$	rhombohedral	<3.79>	24	3×10^{-5}
$NdGaO_3$	tetragonal	<3.84>	24	3×10^{-4}
$SrTiO_3$	cubic	3.905	>>100	$> 10^{-2}$
Sr_2AlTaO_6	cubic	3.895	12	4×10^{-5}
Sr_2AlNbO_6	cubic	3.890	19	2×10^{-5}
MgO	cubic	4.212	9.6	4×10^{-5}
CeO_2	cubic	3.826	16	--
ZrO_2	cubic	3.634	26	8×10^{-3}
(YBCO	orthorhombic	<3.85>	--	--)

that there are electrical shorts. It has also been reported that the presence of an oxygen plasma during the cooldown after the insulator growth is effective in oxidizing the YBCO underneath [24].

Many of the materials listed in Table 1 were first used as substrates for HTS films. Two of the most widely used, for high frequency applications, are lanthanum aluminate, $LaAlO_3$, and neodymium gallate, $NdGaO_3$. $LaAlO_3$ is available in up to 3-inch diameter, and $NdGaO_3$ up to 2-inch. For multilayer devices $LaAlO_3$ is not useful because of twinning. The as-grown crystals are heavily twinned, and after a YBCO film is deposited, typically at 600–800°C, which is above the $LaAlO_3$ structural phase transition, these twins reform in new locations. The resulting distortion leads to the wafer surface becoming rough, and can result in movement of previously patterned features over distances of several microns. This makes alignment of the next layer impossible. For this reason we use $NdGaO_3$ as the substrate for multilayer devices, since its dielectric properties are acceptable, and it can be grown twin-free. In addition, its structural phase transition is at about 1300°C, so that there is no danger of twins forming during film growth.

A recent review of substrate issues is given in reference [25].

4. HTS Josephson Junctions

While numerous approaches have been used to fabricate HTS SNS junctions or weak links, only a few hold the promise of sufficient reproducibility for use in digital circuits. Figure 2 illustrates some of the most promising approaches (from either a practical or theoretical standpoint), which can be grouped into two categories: grain boundary junctions, and SNS junctions with epitaxial normal layers.

4.1. GRAIN BOUNDARY JUNCTIONS

Grain boundary (GB) junctions, rely on the experimental fact that a grain boundary in an HTS films, provided the degree of misorientation is great enough, behaves electrically like an SNS junction or weak link. This was investigated in detail at IBM [26–28], where the dependence of the critical current density, J_c, on misorientation angle was investigated. The grain boundary may be nucleated in an HTS film at a prescribed location such as a grain boundary in the underlying substrate (*bicrystal* junction) or thin-film template (*biepitaxial junctions* [29,30]), or at a step in the substrate (*step-edge grain boundary, or SEGB, junctions)*, as illustrated in Fig. 3(a). The

latter approach actually involves two grain boundaries in series, at the top and bottom of the step, although the critical currents of the two are usually sufficiently different that only the weakest one comes into play in applications [31–37].

The SEGB approach has several merits for use in digital circuits. First, the junctions can be located at arbitrary locations and in any of four crytallographically defined directions with respect to the substrate, since the step locations are typically defined using photolithography and ion milling. This is in contrast to the bicrystal junctions, where the grain boundary location is defined by the fusing of two separate, misoriented pieces of substrate material. Second, the misorientation angle of the grain boundaries fortuitously gives a value of J_c which is in the right range for digital circuits.

A further advantage of the SEGB approach is that is straightforwardly generalized to a multilayer configuration, where the step may be formed in a deposited insulator instead of, or in addition to, in the substrate [38]. Such a process, first demonstrated by us, is discussed in section 5.

Ultimately the simplicity of the SEGB approach is a limitation, in that there are few experimental parameters available to adjust the critical current and resistance values. In particular, the degree of critical current reproducibility, while sufficient for applications such as SQUIDs, is probably too limited for demanding applications such as digital circuits.

Obviously the potential for formation of *unwanted* grain boundaries at steps has ramifications for the patterning of multilayer circuits, as will be discussed in Section 5.

4.2. ALL-EXPITAXIAL SNS JUNCTIONS

A more promising approach in these respects is the *all epitaxial SNS* junction, based on the deliberate formation of a nominally SNS structure, using a normal layer which is structurally and chemically matched to the YBCO superconducting electrodes. Demonstrated normal materials which meet these criteria include $PrBa_2Cu_3O_x$ [39–41], $PrBa_2Cu_{3-x}Ga_xO_y$ [42], non-superconducting YBCO [43], $CaRuO_3$ [44], $SrRuO_3$ [45,46] and various substituted YBCO materials, such as $Y_{1-x}Ca_xBa_2Cu_3O_x$ [47], $Y_{1-x}Pr_xBa_2Cu_3O_x$ [48,49], and $YBa_2Cu_{3-x}Co_xO_x$ [50,51]. The two most common configurations for such all-epitaxial devices are "edge" (or "ramp" or "ramp-edge") junctions, and a-axis trilayer junctions, illustrated in Figure 2

(b) and (c), respectively. Of these the edge SNS junction is by far the most well developed, since it is based on c-axis oriented films, which are easier to fabricate than a-axis.

4.2.1. Edge Junctions

The edge junction is formed by depositing a c-axis oriented HTS film (the

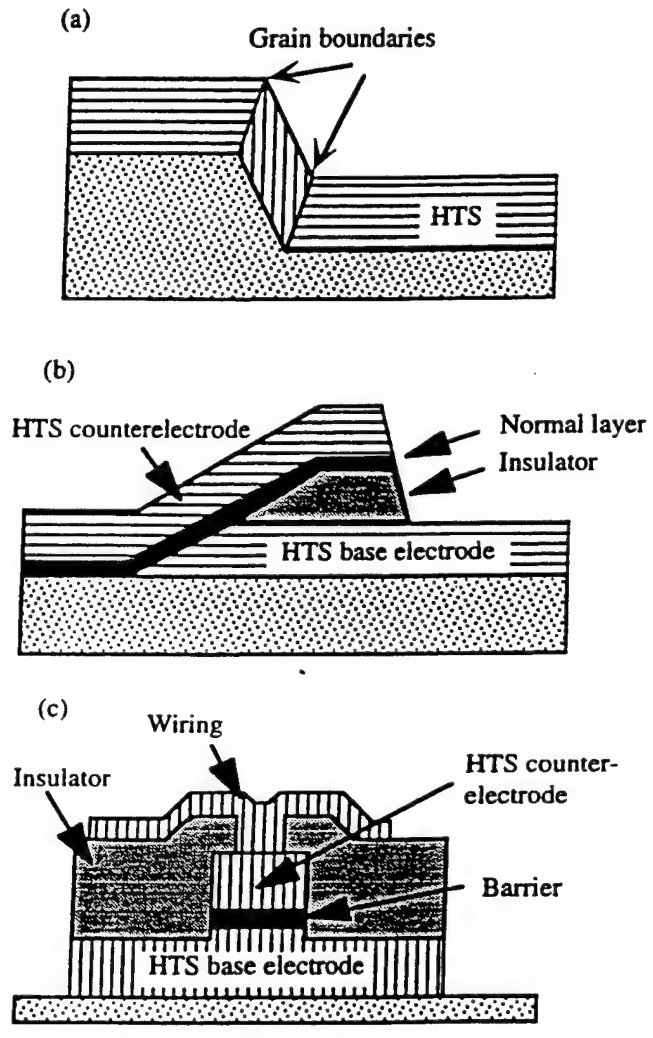

Figure 2. Three types of HTS junctions. (a) Step-edge grain boundary junction (b) Edge, or ramp, SNS junction, and (c) a-axis trilayer junction.

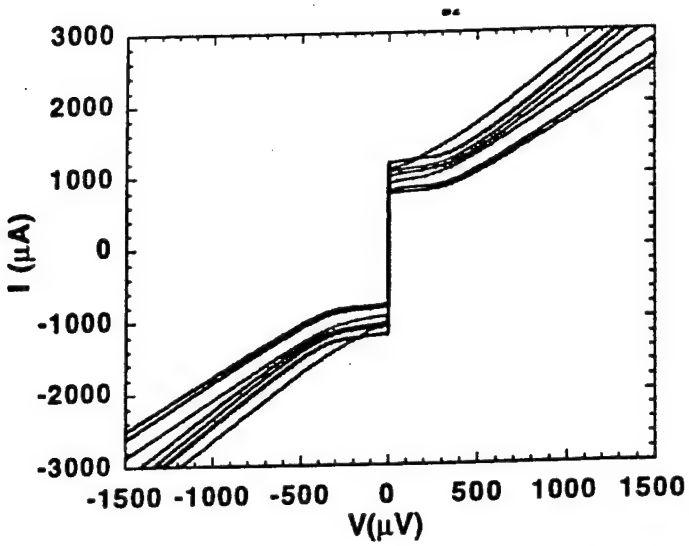

Figure 3. Current voltage characteristics, at 65 K, for eight 4-μm wide SNS edge junctions, with 100 Å $YBa_2Cu_{2.79}Co_{0.21}O_x$ normal metal layer. The uniformity and high I_cR_n (≈ 570 μV) of the junctions is promising for digital circuit applications.

base electrode), followed, usually *in situ*, by an epitaxial insulator. A tapered edge, typically with an angle of 30° or less with respect to the substrate, is formed in this bilayer, commonly by angled ion milling but sometimes by wet-etching [52]. While such a tapered edge is most easily formed by a *unidirectional* milling process, this is generally too restrictive for digital circuits, where it is desirable that junctions be allowed to face in four directions to keep inductances low and allow maximum flexibility in circuit layout. After the edge is formed the sample is cleaned and then the normal layer and top HTS layer, or counterelectrode, are deposited.

Obviously this approach has the disadvantage that one of the key interfaces between superconductor and normal materials is formed *ex-situ*, with the potential for damage associated with ion milling, and formation of a contaminated layer from exposure to air. Ion damage can be quite considerable at typical milling voltages, such as 500eV, producing a disordered layer of order 4 nm thick [53]. The use of extremely low voltages (down to say, 50 eV) can alleviate, though probably not eliminate, this problem. Techniques have also been demonstrated for formation of the edge junction using shadow techniques in an all *in situ* process [54], although they involve directional depositions and are thus probably not flexible

enough for digital circuit fabrication. As for the effects of atmospheric exposure, they can be reduced by an *in situ* ion clean, immediately before the deposition of the normal layer.

Figure 3 shows current-voltage characteristics for eight 4-μm wide SNS edge junctions, with a 100 Å $YBa_2Cu_{2.79}Co_{0.21}O_x$ normal metal layer. They are consistent with the resistively shunted junction (RSJ) model for a low-capacitance SNS or weak link device. The uniformity and high I_cR_n ($\approx$ 570 μV) of the junctions are promising for digital circuit applications. The best such chips have one-sigma spreads in the range of 10–20%, so that, based on Figure 1, circuits with of order 100 junctions should soon be attainable with modest yields.

4.2.2. Trilayer Junctions

An alternative to the c-axis-film-based edge junction is the trilayer junction based on a-axis oriented films, illustrated in Figure 2(c). This junction geometry has the obvious advantage that the key interfaces between superconductor and normal materials can be formed *in situ*, avoiding degradation due to atmospheric exposure or damage associated with ion milling, both of which are unavoidable in the standard edge junction approach. In practice however the relative difficulty of growing high-quality a-axis oriented YBCO films has limited the number of useful demonstrations of this junction geometry. A variant in which (103) oriented YBCO films are used has also been pursued [55].

For circuit use the resistance of such junctions tends to be too low, since the junction size is defined purely lithographically, and thus is typically much larger than that of the edge junction, where one junction dimension is defined by the base electrode film thickness. In addition, the integration of a-axis junctions into a multilayer process will be difficult in that an a-axis oriented YBCO wiring layer connecting the junctions will have very low J_c ($\sim 10^4$ A/cm^2 at 77K, compared to $\sim 10^6$ A/cm^2 for c-axis YBCO), which is too low for most circuits. In fact, because of some of these difficulties of junction integration, there has not been to date even a single demonstration of a dc SQUID based on such junctions.

Thus we consider the most promising junction geometry to be the all-epitaxial edge-geometry SNS junction. Much of the discussion in the rest of the paper will focus on issues related to the integration of such junctions into a useful circuit process, with the attributes discussed in the introduction.

5. Epitaxial Multilayer Circuit Processing

Although the Josephson junction is the single most important element of a superconducting digital circuit, there are numerous other elements which are required to integrate them into a useful circuit, many of which were enumerated in the introduction. Maintaining the required low gate and interconnect inductance in particular requires a superconducting groundplane to be situated as close as possible to the active layers which contain the junctions, which in turn requires a pinhole-free, low-loss insulator between the superconducting layers.

Figure 4 shows schematic cross sections of two multilayer processes which we have used to demonstrate simple HTS digital circuits. The first is a three-epitaxial-layer process which uses SEGB junctions defined at steps etched part way into the deposited $SrTiO_3$ insulator. The second is a six-epitaxial-layer process which incorporates edge SNS junctions, with Co-doped YBCO as the normal layer. In both cases the bottom YBCO layer

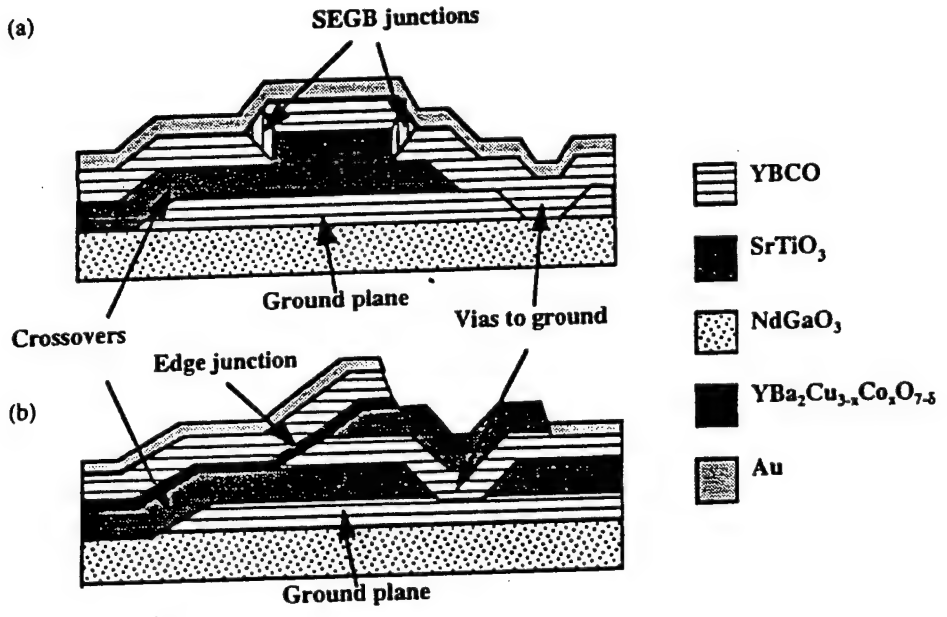

Figure 4. Schematic cross sections of two HTS multilayer processes which we have demonstrated. (a) A three-epitaxial-layer process using SEGB junctions, and (b) a six-epitaxial-layer process using edge SNS junctions.

acts as the ground plane, reducing the inductance of the resulting structures.

In this section we discuss some of the issues involved in building up multiple patterned, epitaxial layers into a useful circuit process. We begin by discussing some generalities about the patterning of such layers.

5.1. FILM PATTERNING

The list of processing techniques used in the fabrication of HTS multilayer devices is a fairly short one. The process, at this state of its development, usually consists of a repeating the following set of steps for each of the epitaxial layers (or in some cases for several layers grown *in situ*): 1) Deposit film(s); 2) Define desired pattern by photolithography; 3) Etch film(s); and 4) Remove resist.

Since the integration density is very low at this stage in the development of HTS digital circuits, the demands on photolithography are minimal, and this is usually adequately performed with contact lithography and standard resists. However, due to the requirement that unwanted grain boundaries not form where on epitaxial film grows over the edge of another, measures are taken to ensure that the photoresist *not* have a steep sidewall. This point is intimately related to the usual etch process which is applied to HTS films, which we discuss next.

In the processing of semiconductor circuits, as well as those based on low temperature superconductors, it is common to use a material-selective reactive ion etch (RIE) process, with fluorine and chlorine based gases. Since the fluorides and chlorides of yttrium, barium, and copper are not volatile at temperatures compatible with resist processing, RIE is not useful for HTS. The principal method is thus ion milling with argon, sometimes with oxygen added. This method allows precise pattern definition, and also allows one to obtain the desired tapered edges in the films, typically by milling with the ion beam at a low angle with respect to the substrates, and usually with the substrates rotating about their normal.

Returning to the issue of photolithography, the profile of the tapered edges of the etched films is strongly affected by the profile of the photoresist, and it is usually advantageous to deliberately taper the resist edges. This can be done by "reflowing" the resist at an elevated temperature (typically from 130°C to 180°C). Also, the use of oxygen in the milling gas will tend to erode the photoresist relatively rapidly, making the resist wall recede during the etching, and thus contributing to the taper.

Wet etches can also be used for the patterning of the YBCO layers. For example, in ref. [52] a bromine-in-alcohol etch, first demonstrated by Vasquez [56], was used to prepare edges in bilayers of PBCO (in this case used as an "insulator") and YBCO for edge junctions. Since the etch rate is highly anisotropic this led to the formation of very shallow tapered edges, about 3° with respect to the substrate. Unfortunately this particular etch is not useful for etching other epitaxial insulators of more interest to HTS digital circuits.

Another technique which has been applied to patterning of HTS films is "lift-off" or "rejection" using a mask of, for example, zirconium oxide on calcium fluoride, which can be dissolved in water after the HTS deposition [57].

Another potentially powerful technique is the use of ion-implantation, to selectively transform regions of an HTS film into an insulator. This has the advantage of leaving a completely planar surface, with no edges at which unwanted grain boundaries might nucleate. Such a process has not yet been used to fabricate a complex multilayer device.

5.2. PREPARATION FOR SUBSEQUENT EPITAXIAL GROWTH

There are two factors that necessitate extreme care when preparing a previously deposited and patterned YBCO layer for the growth of an epitaxial overlayer, such as an insulator or another YBCO layer. First YBCO is very reactive, so that a degraded surface layer can form even upon a short exposure to air, and particularly upon processing with photoresist. This layer typically consists of hydroxides, carbonates such as $BaCO_3$ [56], and hydrocarbons. To ensure high-quality epitaxial overgrowth it is essential to remove this degraded layer. Failure to do so typically leads to subsequent YBCO layers having inferior superconducting properties, and having a large density of defects in the form of Cu-rich second phase particles, or "boulders" which can protrude from the surface by as much as a micron. These can then in turn lead to electrical shorts through insulator films grown over them.

In practice we find that the surface of a patterned YBCO layer is best cleaned of a reacted surface layer by some combination of oxygen plasma, which is very effective in removing hydrocarbons, and ion milling, which etches the surface relatively unselectively. XPS studies of the YBCO surfaces show that carbon peaks caused by exposure to air and to photoresist are completely suppressed when the surface is given a treatment of oxygen

plasma, acetone rinse, second oxygen plasma, and then heating to deposition temperature (≈ 700°C) in the sputter gas mixture of argon and oxygen [23].

5.3. INSULATOR INTEGRITY

Any of the deposition methods discussed earlier is capable of producing insulators with low pinhole density. In ref. [58] we reported a series of experiments to determine which process parameters had the greatest effect on whether a minimum electrical isolation of 2×10^4 Ω-cm was achieved in YBCO/insulator/YBCO trilayer capacitors, using both $SrTiO_3$ and Sr_2AlTaO_6. It was found that such factors as the insulator growth temperature in the range of 660-750°C, whether the layers were deposited without breaking vacuum, interfaces exposed to air, or interfaces exposed to ion-mill processing, were not significant.

Roughness of the first YBCO layer was found to be the key factor in determining electrical isolation Measurements of the resistance of capacitor structures typically yielded effective resitivities in the 10^8–10^9 Ω-cm range, which is well above the minimum resistivity requirement of ~ 10^4 Ω-cm which we have estimated for high speed digital circuits [23], as long as there was a sufficiently low density (~ 10^2 cm^{-2} or less) of outgrowths in the bottom YBCO layer.

The disruptive potential of these outgrowths is well illustrated by Figure 5, which shows a cross-sectional TEM image of an SNS edge junction, with a

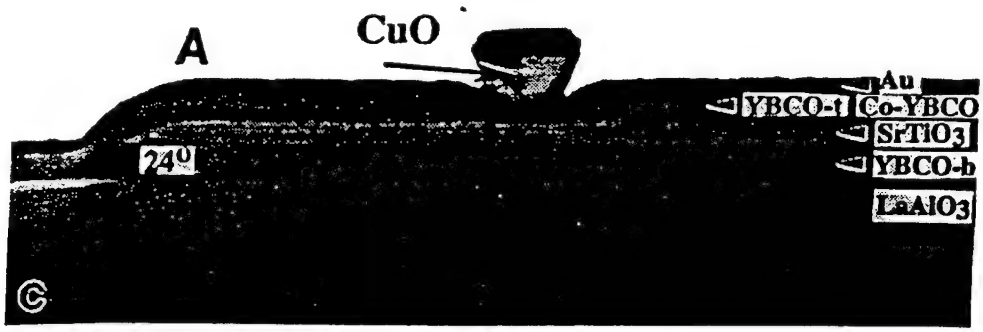

Figure 5. Cross-sectional TEM of an HTS edge junction, showing a CuO "boulder" growing in the top YBCO layer. The presence of such outgrowth in the bottom YBCO layer would typically cause a short through the insulator.

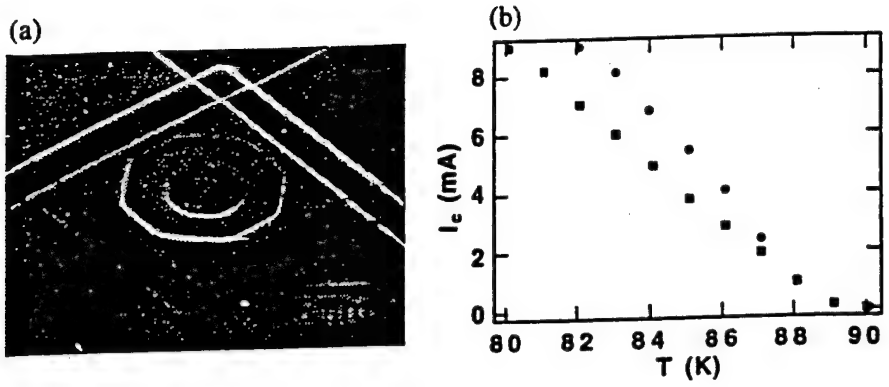

Figure 6. (a) A superconducting via between two YBCO layers. The inner circle is a hole in the bottom YBCO layer to allow a-b-axis contact between the two layers, while the hexagon is the hole through the $SrTiO_3$ insulator. (b) Critical current vs. temperature for a series array of twelve such vias.

CuO boulder in the top layer. Clearly the presence of such outgrowth in the bottom layer would disrupt the growth of the insulator, and potentially cause a short.

5.4. CROSSOVER AND VIA STRUCTURES

If precautions are taken to ensure that all edges are suitably tapered, as discussed above, then it is generally straightforward to produce crossover structures (where a top HTS films crosses a pattern in the underlying insulator and/or HTS films) and vias (holes in the insulator through which two HTS films contact each other). Crossover J_c's in the 10^5 A/cm^2 range at 77 K are easily obtained [23], while values above 10^6 A/cm^2 have been obtained by use of a novel combination of wet etching and ion milling [59]. The use of planarization techniques potentially allows for essentially no degradation in J_c compared to a "flat" film [60].

Figure 6 shows a scanning electron micrograph of a typical via structure where two crossed YBCO strips contact each other through a hole in the intervening $SrTiO_3$. There is both a-b-axis and c-axis contact between YBCO layers because a hole has been patterned in the bottom YBCO, interior to the hole in the $SrTiO_3$. Figure 6(b) shows data for I_c versus temperature for a series array of twelve such vias. The values obtained are well above junction I_c's of interest, and therefore should not be a limitation.

5.5. JUNCTIONS & SQUIDS IN MULTILAYERS

We have fabricated and characterized SQUIDs with integrated YBCO ground planes using the multilayer SEGB [38] and SNS [61,62] processes of Figure 4. The properties of the junctions are usually found to be comparable to those fabricated without a ground plane, as long as the ground plane is sufficiently smooth.

Inductance measurements on the SQUIDs yield values of about 1 pH per square at 65 K, which is low enough to be useful for digital circuits, although obtaining a total SQUID inductance as low as 4 pH, as discussed in the introduction, is still a design challenge.

5.6. MULTILAYER HTS CIRCUITS

We have also fabricated some simple circuits, with up to ten junctions, using the multilayer processes — to our knowledge the first all-HTS multilayer digital circuits. The most complex, a 1-bit A/D converter is shown in Figure 7, in the SNS version, and was operated successfully at low speed at 65 K [63]. A version based on SEGB JJs was operated up to 60 K.

Other demonstrated circuits include Set-Reset flip-flops and an SFQ-to-dc converter operated at low speed, and a Toggle flip-flop operating correctly, on average, up to 15 GHz.

6. Conclusions

There are numerous challenges before us if we are to realize the great potential of HTS digital circuits, the most significant of which is to improve the control, on-chip, chip-to-chip, and run-to-run, of junction critical currents. We believe that the best prospects for this lie with edge-geometry SNS junctions, where spreads approaching 10%, one-sigma, have been observed for as many as twenty junctions.

Further optimization will involve better control of film properties, including surface morphology, which can have a profound effect on junction properties — especially when junctions are fabricated on top of a ground plane. Investigation of new normal-layer materials may also be fruitful, as will more detailed investigation of the formation of the ramp edge, and the

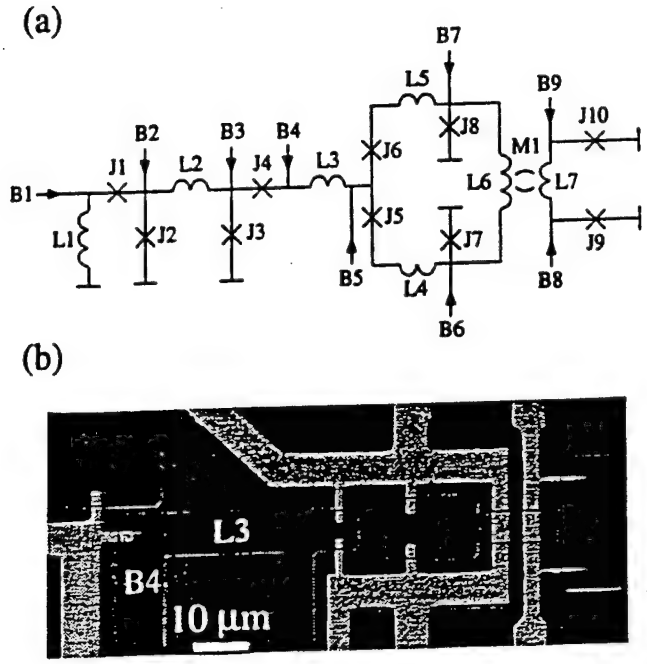

Figure 7. Circuit schematic, (a), and optical micrograph, (b), of a multilayer HTS 1-bit analog to digital converter, fabricated using SNS edge junctions. The circuit was operated successfully at 65 K.

growth on that edge. Multilayer configurations with the ground plane on the top of the junctions, which we have recently demonstrated, also require further study, since there are obvious advantages to forming the junctions on the smoothest possible surface — the substrate.

Most of the multilayer work done to date has used $SrTiO_3$ or $PrBa_2Cu_3O_x$ as the deposited insulator, both of which are probably too lossy for high frequency applications. Recently, however, a multilayer junction process incorporating low-loss $Sr_2AlNbO_6$was demonstrated at Conductus [64]. Further development of low-loss insulators is required.

Much of the development of epitaxial multilayer devices has been driven by the need for SQUIDs for magnetic sensing. However, SQUID applications do not have stringent requirements on junction uniformity, so the impetus for improvements in this area must come from the development of a market for HTS digital products, such as high-resolution and high speed ADCs, network switches, and digital signal processors.

Although the pace of semiconductor development is relentless, we believe that there will be a place for the unique capabilities of a fully developed HTS digital technology.

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Materials Basis for a Six-Level Epitaxial HTS Digital Circuit Process

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Abstract — **We have developed a process for fabrication of HTS single-flux-quantum logic circuits based on edge SNS junctions which requires six epitaxial film layers and six mask levels. The process was successfully applied to fabrication of small-scale circuits (≤ 10 junctions). This paper examines the materials properties affecting the reproducibility of YBCO-based SNS junctions, the low inductance provided by an integrated YBCO ground plane, and electrical isolation by $SrTiO_3$ or Sr_2AlTaO_6 ground-plane and junction insulator layers. Some of the critical processing parameters identified by electrical measurements, TEM, SEM, and AFM were control of second-phase precipitates in YBCO, oxygen diffusion, Ar ion-milling parameters, and preparation of surfaces for subsequent high-temperature depositions.**

I. Introduction

Practical application of Single Flux Quantum (SFQ) logic circuits fabricated in High-T_c Superconductors (HTS) is limited at present by a low level of integration of Josephson junctions with sufficiently uniform characteristics. SFQ gates must have a low inductance, L, consistent with a quantum of flux, $LI_c \sim \Phi_o = 2$ mA-pH, and a Josephson critical current, I_c, on the order of 0.5 mA for thermal noise stability. Two approaches for achieving such low inductances are to use an integrated thin-film HTS groundplane or to use submicron lithography. We chose to follow the former approach in the process described here.

The requirements for junction reproducibility are shown in Fig. 1 following the discussion in [1]. Reproducibility is expressed as the standard deviation of Josephson critical currents, I_c. The calculation of junction count for a particular level of junction reproducibility assumes a Gaussian distribution of critical currents, and circuit component margins of 30%, which have been shown to be realistic in both simulations and LTS circuit measurements for SFQ circuits. Since there is always some chance with a Gaussian distribution that a junction's I_c will fall outside of circuit margins, circuit yield is expected to be < 100% even for small-scale circuits with low junction counts.

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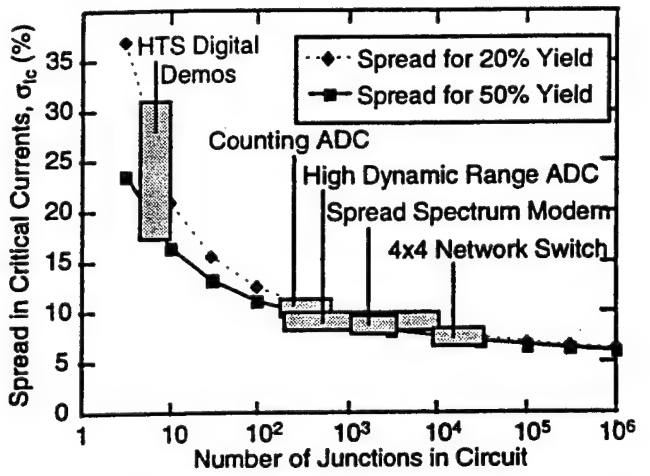

Fig. 1. The spread in junction critical currents, σ_{Ic}, required to produce circuits with a given junction count. Small-scale circuit demonstrations made to date are consistent with relatively large spreads in I_c of 20-30%. To fabricate SFQ circuits of practical interest with hundreds to thousands of junctions and reasonable yields, I_c spreads must be reduced to ≤ 10%.

Fig. 1 shows that one should expect no more than the small-scale SFQ circuit demonstrations made to date as long as σ_{Ic} = 20-30%. To fabricate circuits of practical interest with hundreds to thousands of junctions and reasonable yields, I_c spreads must be reduced to ≤ 10% while still satisfying the requirement for $LI_c \sim \Phi_o$.

Details are published elsewhere of junction electrical properties and some process issues [2-3], inductance measurements [4], and one of the circuits fabricated with this process [5]. The emphasis of this paper is in showing how the materials properties needed for groundplane integration and improved junction reproducibility are affected by the details of our integrated circuit fabrication process. Although the number of essential film layers is exactly the same, it is important to distinguish the multilayer film process for HTS digital circuits described here from that needed for integrating magnetometer pick-up coils with SQUIDs as in [6]. In the case of magnetometers, there is a minimal overlap of YBCO film layers which occurs only at crossovers. Junctions are fabricated directly on the substrate.

II. Integrated Circuit Fabrication Process

Major process steps we followed to integrate edge SNS junctions on an HTS groundplane are shown in Fig. 2. A minimum of six mask levels and six epitaxial oxide film

layers are needed for this process. Two additional epitaxial film layers were sometimes used, a 300 Å $SrTiO_3$ (STO) buffer layer between the substrate and groundplane, and a 300 Å STO cap layer deposited on top of the groundplane to protect the YBCO surface during processing. Since neither the presence or absence of these layers affected the sequence of process steps, we omitted them from the schematic cross sections of multilayers. Next we will describe in detail each of the six steps shown in Fig. 2.

A. Groundplane Deposition and Patterning

YBCO groundplane films 2250 Å thick were deposited by 90° off-axis rf magnetron sputtering with a process described in [7]. In all cases, $NdGaO_3$(110) substrates were used. In some cases, 2-inch diameter wafers were used which were diced into 1 cm × 1 cm chips at some point before circuit fabrication was completed so deposition parameters for the junction films could be varied while keeping groundplane fabrication parameters constant.

Fig. 3 shows the mask layout for (3a) a wafer, (3b) a chip, and (3c) a standard junction test subchip. The dark band on the subchip is the base electrode with two wire bond pads. The rest of the bonding pads are connected in pairs to the top electrodes of 20 devices. The edge SNS devices face in all four in-plane directions since this is a constraint imposed by the need for low-inductance connections in SFQ circuits. Junctions are spread out across each subchip to give a more complete measurement of junction uniformity.

Film patterning was done with photoresist masks reflowed for 5 min at 130°C. Wafers were tilted 50° from normal and rotated during 150 eV Ar ion milling to produce edges that angled 20-30° from the substrate plane. The same process was used to pattern single or multiple layers. SIMS endpoint detection prevented over-milling.

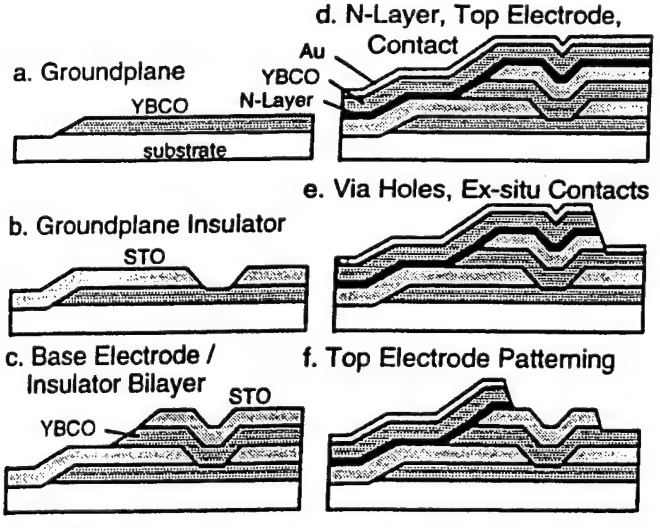

Fig. 2. The major process steps for fabrication of SFQ circuits with SNS junctions integrated on grounplanes for low inductance. The effect of each step on materials properties critical for groundplane integration and junction reproducibility are described in the text.

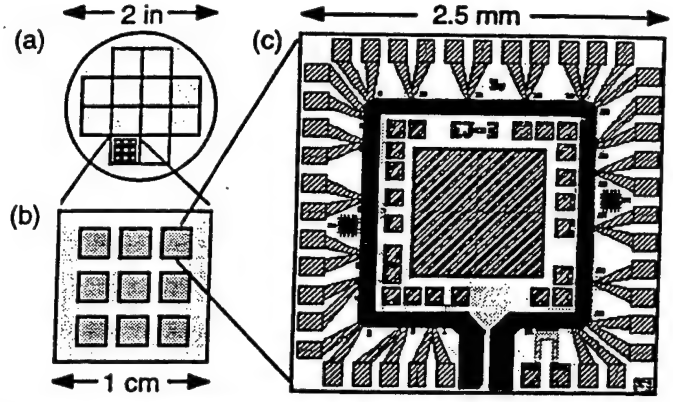

Fig. 3. YBCO groundplanes were deposited and patterned on 2-inch wafers (a) which were diced into 1 cm × 1 cm chips (b) for deposition of subsequent layers. Each chip had nine subchips where (c) was one of our standard patterns for measurement of twenty 3-μm-wide devices.

B. Groundplane Insulator Deposition and Patterning

Before we brought any patterned wafer up to ~700°C for deposition of a subsequent epitaxial layer, we cleaned the surface with an *ex-situ* oxygen plasma and a 150 eV Ar/O_2 ion mill to remove ~100 Å from the surface. XPS studies were used to ensure that hydrocarbon and fluorine residues were completely removed by the time the sample was brought to the desired deposition temperature [8].

Both $SrTiO_3$ and Sr_2AlTaO_6 (SAT) grown by off-axis sputtering were developed for epitaxial insulator films. Groundplane insulators were nominally 2400 Å thick but films used for insulator development varied in thickness between 1000 Å and 3000 Å without apparent thickness dependence. The important properties for the groundplane insulator were good electrical isolation and vias to ground capable of carrying currents greater than the junction critical currents (Fig. 2b).

A series of experiments were performed to determine which process parameters had the greatest effect on whether a minimum electrical isolation of 2×10^4 Ω-cm was achieved in YBCO/insulator/YBCO trilayer capacitors. We found that the insulator growth temperature in the range of 660-750°C, whether the layers were deposited without breaking vacuum, interfaces exposed to air, or interfaces exposed to ion-mill processing, were not significant factors. We also found that room temperature measurements were good predictors of isolation at 77K.

However, roughness of the first YBCO layer was found to be the key factor in determining electrical isolation. Fig. 4 shows the defect density in insulators inferred from the fraction of 35 capacitors per chip ranging in area from 1 mm × 1 mm to 250 μm × 250 μm. In [9], the defect density, D, is calculated from the "yield," the fraction of capacitors exceeding the minimum resistivity criterion, based on,

$$\text{yield} = (\#\ \text{working}) / (\#\ \text{tested}) = \exp(-D / \text{Area}) \qquad (1)$$

latter approach actually involves two grain boundaries in series, at the top and bottom of the step, although the critical currents of the two are usually sufficiently different that only the weakest one comes into play in applications [31–37].

The SEGB approach has several merits for use in digital circuits. First, the junctions can be located at arbitrary locations and in any of four crytallographically defined directions with respect to the substrate, since the step locations are typically defined using photolithography and ion milling. This is in contrast to the bicrystal junctions, where the grain boundary location is defined by the fusing of two separate, misoriented pieces of substrate material. Second, the misorientation angle of the grain boundaries fortuitously gives a value of J_c which is in the right range for digital circuits.

A further advantage of the SEGB approach is that is straightforwardly generalized to a multilayer configuration, where the step may be formed in a deposited insulator instead of, or in addition to, in the substrate [38]. Such a process, first demonstrated by us, is discussed in section 5.

Ultimately the simplicity of the SEGB approach is a limitation, in that there are few experimental parameters available to adjust the critical current and resistance values. In particular, the degree of critical current reproducibility, while sufficient for applications such as SQUIDs, is probably too limited for demanding applications such as digital circuits.

Obviously the potential for formation of *unwanted* grain boundaries at steps has ramifications for the patterning of multilayer circuits, as will be discussed in Section 5.

4.2. ALL-EXPITAXIAL SNS JUNCTIONS

A more promising approach in these respects is the *all epitaxial SNS* junction, based on the deliberate formation of a nominally SNS structure, using a normal layer which is structurally and chemically matched to the YBCO superconducting electrodes. Demonstrated normal materials which meet these criteria include $PrBa_2Cu_3O_x$ [39–41], $PrBa_2Cu_{3-x}Ga_xO_y$ [42], non-superconducting YBCO [43], $CaRuO_3$ [44], $SrRuO_3$ [45,46] and various substituted YBCO materials, such as $Y_{1-x}Ca_xBa_2Cu_3O_x$ [47], $Y_{1-x}Pr_xBa_2Cu_3O_x$ [48,49], and $YBa_2Cu_{3-x}Co_xO_x$ [50,51]. The two most common configurations for such all-epitaxial devices are "edge" (or "ramp" or "ramp-edge") junctions, and a-axis trilayer junctions, illustrated in Figure 2

(b) and (c), respectively. Of these the edge SNS junction is by far the most well developed, since it is based on c-axis oriented films, which are easier to fabricate than a-axis.

4.2.1. Edge Junctions

The edge junction is formed by depositing a c-axis oriented HTS film (the

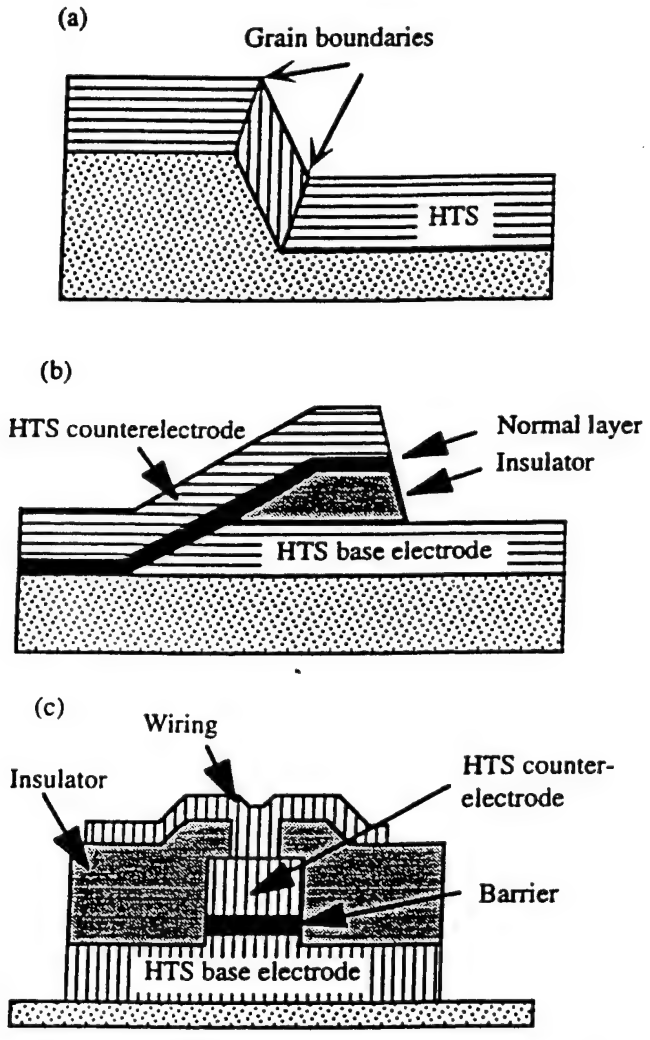

Figure 2. Three types of HTS junctions. (a) Step-edge grain boundary junction (b) Edge, or ramp, SNS junction, and (c) a-axis trilayer junction.

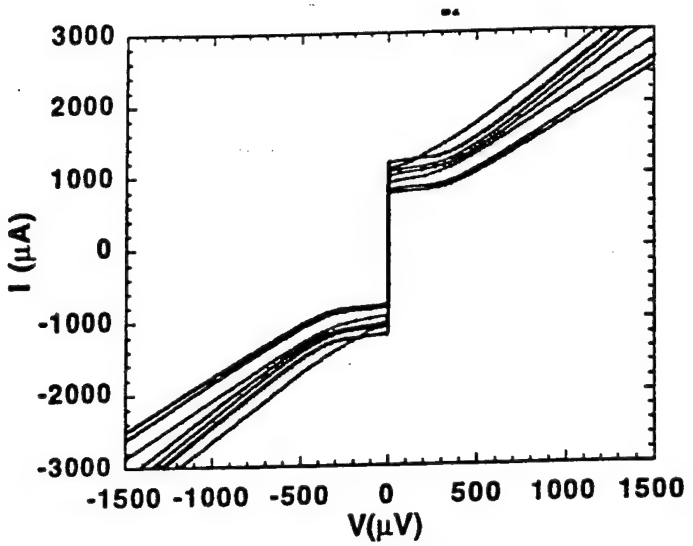

Figure 3. Current voltage characteristics, at 65 K, for eight 4-μm wide SNS edge junctions, with 100 Å $YBa_2Cu_{2.79}Co_{0.21}O_x$ normal metal layer. The uniformity and high I_cR_n (≈ 570 μV) of the junctions is promising for digital circuit applications.

base electrode), followed, usually *in situ*, by an epitaxial insulator. A tapered edge, typically with an angle of 30° or less with respect to the substrate, is formed in this bilayer, commonly by angled ion milling but sometimes by wet-etching [52]. While such a tapered edge is most easily formed by a *unidirectional* milling process, this is generally too restrictive for digital circuits, where it is desirable that junctions be allowed to face in four directions to keep inductances low and allow maximum flexibility in circuit layout. After the edge is formed the sample is cleaned and then the normal layer and top HTS layer, or counterelectrode, are deposited.

Obviously this approach has the disadvantage that one of the key interfaces between superconductor and normal materials is formed *ex-situ*, with the potential for damage associated with ion milling, and formation of a contaminated layer from exposure to air. Ion damage can be quite considerable at typical milling voltages, such as 500eV, producing a disordered layer of order 4 nm thick [53]. The use of extremely low voltages (down to say, 50 eV) can alleviate, though probably not eliminate, this problem. Techniques have also been demonstrated for formation of the edge junction using shadow techniques in an all *in situ* process [54], although they involve directional depositions and are thus probably not flexible

enough for digital circuit fabrication. As for the effects of atmospheric exposure, they can be reduced by an *in situ* ion clean, immediately before the deposition of the normal layer.

Figure 3 shows current-voltage characteristics for eight 4-μm wide SNS edge junctions, with a 100 Å $YBa_2Cu_{2.79}Co_{0.21}O_x$ normal metal layer. They are consistent with the resistively shunted junction (RSJ) model for a low-capacitance SNS or weak link device. The uniformity and high I_cR_n (≈ 570 μV) of the junctions are promising for digital circuit applications. The best such chips have one-sigma spreads in the range of 10–20%, so that, based on Figure 1, circuits with of order 100 junctions should soon be attainable with modest yields.

4.2.2. Trilayer Junctions

An alternative to the c-axis-film-based edge junction is the trilayer junction based on a-axis oriented films, illustrated in Figure 2(c). This junction geometry has the obvious advantage that the key interfaces between superconductor and normal materials can be formed *in situ*, avoiding degradation due to atmospheric exposure or damage associated with ion milling, both of which are unavoidable in the standard edge junction approach. In practice however the relative difficulty of growing high-quality a-axis oriented YBCO films has limited the number of useful demonstrations of this junction geometry. A variant in which (103) oriented YBCO films are used has also been pursued [55].

For circuit use the resistance of such junctions tends to be too low, since the junction size is defined purely lithographically, and thus is typically much larger than that of the edge junction, where one junction dimension is defined by the base electrode film thickness. In addition, the integration of a-axis junctions into a multilayer process will be difficult in that an a-axis oriented YBCO wiring layer connecting the junctions will have very low J_c (~ 10^4 A/cm^2 at 77K, compared to ~10^6 A/cm^2 for c-axis YBCO), which is too low for most circuits. In fact, because of some of these difficulties of junction integration, there has not been to date even a single demonstration of a dc SQUID based on such junctions.

Thus we consider the most promising junction geometry to be the all-epitaxial edge-geometry SNS junction. Much of the discussion in the rest of the paper will focus on issues related to the integration of such junctions into a useful circuit process, with the attributes discussed in the introduction.

5. Epitaxial Multilayer Circuit Processing

Although the Josephson junction is the single most important element of a superconducting digital circuit, there are numerous other elements which are required to integrate them into a useful circuit, many of which were enumerated in the introduction. Maintaining the required low gate and interconnect inductance in particular requires a superconducting groundplane to be situated as close as possible to the active layers which contain the junctions, which in turn requires a pinhole-free, low-loss insulator between the superconducting layers.

Figure 4 shows schematic cross sections of two multilayer processes which we have used to demonstrate simple HTS digital circuits. The first is a three-epitaxial-layer process which uses SEGB junctions defined at steps etched part way into the deposited $SrTiO_3$ insulator. The second is a six-epitaxial-layer process which incorporates edge SNS junctions, with Co-doped YBCO as the normal layer. In both cases the bottom YBCO layer

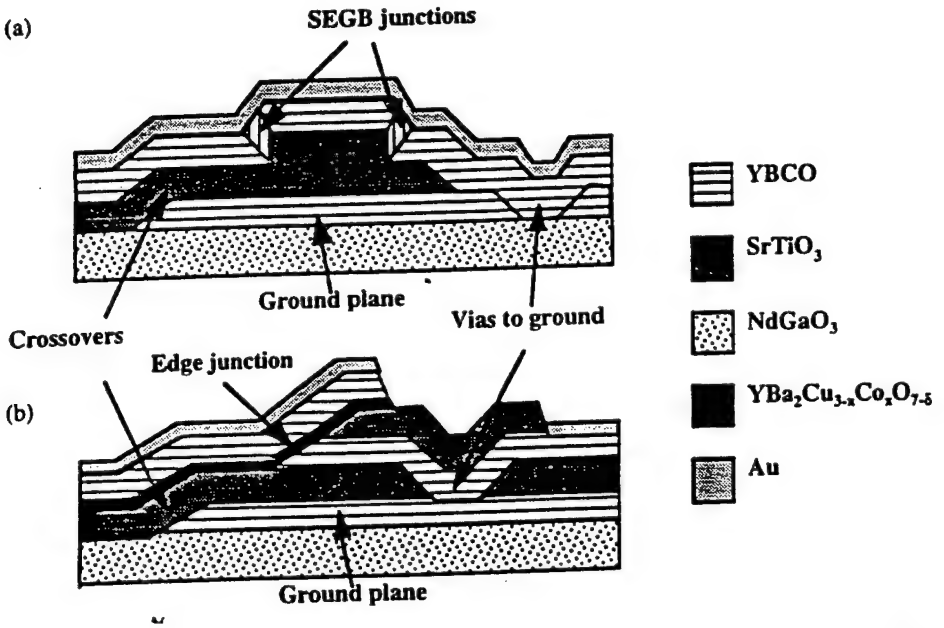

Figure 4. Schematic cross sections of two HTS multilayer processes which we have demonstrated. (a) A three-epitaxial-layer process using SEGB junctions, and (b) a six-epitaxial-layer process using edge SNS junctions.

acts as the ground plane, reducing the inductance of the resulting structures.

In this section we discuss some of the issues involved in building up multiple patterned, epitaxial layers into a useful circuit process. We begin by discussing some generalities about the patterning of such layers.

5.1. FILM PATTERNING

The list of processing techniques used in the fabrication of HTS multilayer devices is a fairly short one. The process, at this state of its development, usually consists of a repeating the following set of steps for each of the epitaxial layers (or in some cases for several layers grown *in situ*): 1) Deposit film(s); 2) Define desired pattern by photolithography; 3) Etch film(s); and 4) Remove resist.

Since the integration density is very low at this stage in the development of HTS digital circuits, the demands on photolithography are minimal, and this is usually adequately performed with contact lithography and standard resists. However, due to the requirement that unwanted grain boundaries not form where on epitaxial film grows over the edge of another, measures are taken to ensure that the photoresist *not* have a steep sidewall. This point is intimately related to the usual etch process which is applied to HTS films, which we discuss next.

In the processing of semiconductor circuits, as well as those based on low temperature superconductors, it is common to use a material-selective reactive ion etch (RIE) process, with fluorine and chlorine based gases. Since the fluorides and chlorides of yttrium, barium, and copper are not volatile at temperatures compatible with resist processing, RIE is not useful for HTS. The principal method is thus ion milling with argon, sometimes with oxygen added. This method allows precise pattern definition, and also allows one to obtain the desired tapered edges in the films, typically by milling with the ion beam at a low angle with respect to the substrates, and usually with the substrates rotating about their normal.

Returning to the issue of photolithography, the profile of the tapered edges of the etched films is strongly affected by the profile of the photoresist, and it is usually advantageous to deliberately taper the resist edges. This can be done by "reflowing" the resist at an elevated temperature (typically from 130°C to 180°C). Also, the use of oxygen in the milling gas will tend to erode the photoresist relatively rapidly, making the resist wall recede during the etching, and thus contributing to the taper.

Wet etches can also be used for the patterning of the YBCO layers. For example, in ref. [52] a bromine-in-alcohol etch, first demonstrated by Vasquez [56], was used to prepare edges in bilayers of PBCO (in this case used as an "insulator") and YBCO for edge junctions. Since the etch rate is highly anisotropic this led to the formation of very shallow tapered edges, about 3° with respect to the substrate. Unfortunately this particular etch is not useful for etching other epitaxial insulators of more interest to HTS digital circuits.

Another technique which has been applied to patterning of HTS films is "lift-off" or "rejection" using a mask of, for example, zirconium oxide on calcium fluoride, which can be dissolved in water after the HTS deposition [57].

Another potentially powerful technique is the use of ion-implantation, to selectively transform regions of an HTS film into an insulator. This has the advantage of leaving a completely planar surface, with no edges at which unwanted grain boundaries might nucleate. Such a process has not yet been used to fabricate a complex multilayer device.

5.2. PREPARATION FOR SUBSEQUENT EPITAXIAL GROWTH

There are two factors that necessitate extreme care when preparing a previously deposited and patterned YBCO layer for the growth of an epitaxial overlayer, such as an insulator or another YBCO layer. First YBCO is very reactive, so that a degraded surface layer can form even upon a short exposure to air, and particularly upon processing with photoresist. This layer typically consists of hydroxides, carbonates such as $BaCO_3$ [56], and hydrocarbons. To ensure high-quality epitaxial overgrowth it is essential to remove this degraded layer. Failure to do so typically leads to subsequent YBCO layers having inferior superconducting properties, and having a large density of defects in the form of Cu-rich second phase particles, or "boulders" which can protrude from the surface by as much as a micron. These can then in turn lead to electrical shorts through insulator films grown over them.

In practice we find that the surface of a patterned YBCO layer is best cleaned of a reacted surface layer by some combination of oxygen plasma, which is very effective in removing hydrocarbons, and ion milling, which etches the surface relatively unselectively. XPS studies of the YBCO surfaces show that carbon peaks caused by exposure to air and to photoresist are completely suppressed when the surface is given a treatment of oxygen

plasma, acetone rinse, second oxygen plasma, and then heating to deposition temperature (≈ 700°C) in the sputter gas mixture of argon and oxygen [23].

5.3. INSULATOR INTEGRITY

Any of the deposition methods discussed earlier is capable of producing insulators with low pinhole density. In ref. [58] we reported a series of experiments to determine which process parameters had the greatest effect on whether a minimum electrical isolation of 2×10^4 Ω-cm was achieved in YBCO/insulator/YBCO trilayer capacitors, using both $SrTiO_3$ and Sr_2AlTaO_6. It was found that such factors as the insulator growth temperature in the range of 660-750°C, whether the layers were deposited without breaking vacuum, interfaces exposed to air, or interfaces exposed to ion-mill processing, were not significant.

Roughness of the first YBCO layer was found to be the key factor in determining electrical isolation Measurements of the resistance of capacitor structures typically yielded effective resitivities in the 10^8–10^9 Ω-cm range, which is well above the minimum resistivity requirement of ~ 10^4 Ω-cm which we have estimated for high speed digital circuits [23], as long as there was a sufficiently low density (~ 10^2 cm^{-2} or less) of outgrowths in the bottom YBCO layer.

The disruptive potential of these outgrowths is well illustrated by Figure 5, which shows a cross-sectional TEM image of an SNS edge junction, with a

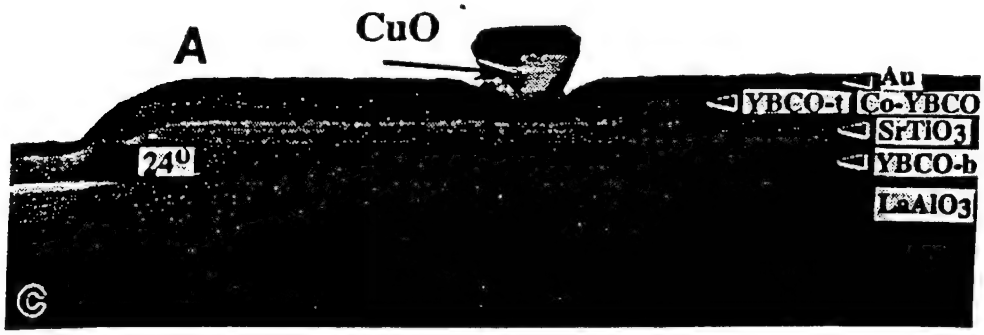

Figure 5. Cross-sectional TEM of an HTS edge junction, showing a CuO "boulder" growing in the top YBCO layer. The presence of such outgrowth in the bottom YBCO layer would typically cause a short through the insulator.

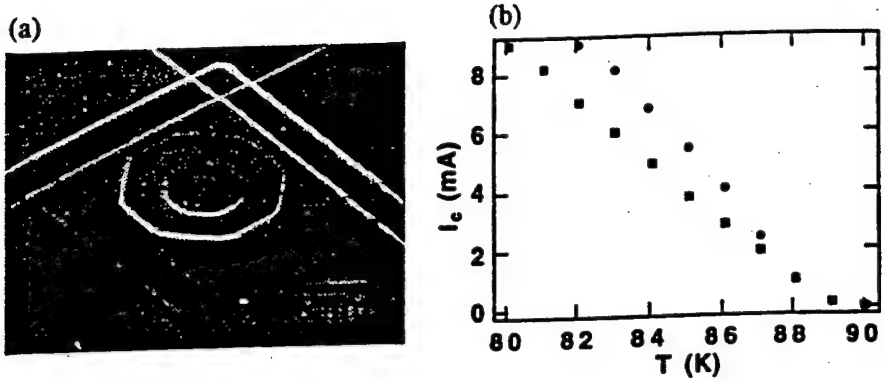

Figure 6. (a) A superconducting via between two YBCO layers. The inner circle is a hole in the bottom YBCO layer to allow a-b-axis contact between the two layers, while the hexagon is the hole through the $SrTiO_3$ insulator. (b) Critical current vs. temperature for a series array of twelve such vias.

CuO boulder in the top layer. Clearly the presence of such outgrowth in the bottom layer would disrupt the growth of the insulator, and potentially cause a short.

5.4. CROSSOVER AND VIA STRUCTURES

If precautions are taken to ensure that all edges are suitably tapered, as discussed above, then it is generally straightforward to produce crossover structures (where a top HTS films crosses a pattern in the underlying insulator and/or HTS films) and vias (holes in the insulator through which two HTS films contact each other). Crossover J_c's in the 10^5 A/cm^2 range at 77 K are easily obtained [23], while values above 10^6 A/cm^2 have been obtained by use of a novel combination of wet etching and ion milling [59]. The use of planarization techniques potentially allows for essentially no degradation in J_c compared to a "flat" film [60].

Figure 6 shows a scanning electron micrograph of a typical via structure where two crossed YBCO strips contact each other through a hole in the intervening $SrTiO_3$. There is both a-b-axis and c-axis contact between YBCO layers because a hole has been patterned in the bottom YBCO, interior to the hole in the $SrTiO_3$. Figure 6(b) shows data for I_c versus temperature for a series array of twelve such vias. The values obtained are well above junction I_c's of interest, and therefore should not be a limitation.

5.5. JUNCTIONS & SQUIDS IN MULTILAYERS

We have fabricated and characterized SQUIDs with integrated YBCO ground planes using the multilayer SEGB [38] and SNS [61,62] processes of Figure 4. The properties of the junctions are usually found to be comparable to those fabricated without a ground plane, as long as the ground plane is sufficiently smooth.

Inductance measurements on the SQUIDs yield values of about 1 pH per square at 65 K, which is low enough to be useful for digital circuits, although obtaining a total SQUID inductance as low as 4 pH, as discussed in the introduction, is still a design challenge.

5.6. MULTILAYER HTS CIRCUITS

We have also fabricated some simple circuits, with up to ten junctions, using the multilayer processes — to our knowledge the first all-HTS multilayer digital circuits. The most complex, a 1-bit A/D converter is shown in Figure 7, in the SNS version, and was operated successfully at low speed at 65 K [63]. A version based on SEGB JJs was operated up to 60 K.

Other demonstrated circuits include Set-Reset flip-flops and an SFQ-to-dc converter operated at low speed, and a Toggle flip-flop operating correctly, on average, up to 15 GHz.

6. Conclusions

There are numerous challenges before us if we are to realize the great potential of HTS digital circuits, the most significant of which is to improve the control, on-chip, chip-to-chip, and run-to-run, of junction critical currents. We believe that the best prospects for this lie with edge-geometry SNS junctions, where spreads approaching 10%, one-sigma, have been observed for as many as twenty junctions.

Further optimization will involve better control of film properties, including surface morphology, which can have a profound effect on junction properties — especially when junctions are fabricated on top of a ground plane. Investigation of new normal-layer materials may also be fruitful, as will more detailed investigation of the formation of the ramp edge, and the

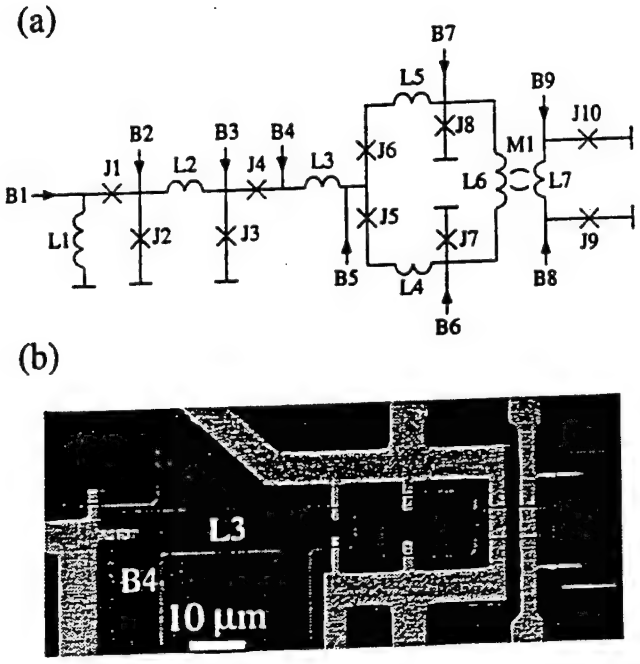

Figure 7. Circuit schematic, (a), and optical micrograph, (b), of a multilayer HTS 1-bit analog to digital converter, fabricated using SNS edge junctions. The circuit was operated successfully at 65 K.

growth on that edge. Multilayer configurations with the ground plane on the top of the junctions, which we have recently demonstrated, also require further study, since there are obvious advantages to forming the junctions on the smoothest possible surface — the substrate.

Most of the multilayer work done to date has used $SrTiO_3$ or $PrBa_2Cu_3O_x$ as the deposited insulator, both of which are probably too lossy for high frequency applications. Recently, however, a multilayer junction process incorporating low-loss $Sr_2AlNbO_6$was demonstrated at Conductus [64]. Further development of low-loss insulators is required.

Much of the development of epitaxial multilayer devices has been driven by the need for SQUIDs for magnetic sensing. However, SQUID applications do not have stringent requirements on junction uniformity, so the impetus for improvements in this area must come from the development of a market for HTS digital products, such as high-resolution and high speed ADCs, network switches, and digital signal processors.

Although the pace of semiconductor development is relentless, we believe that there will be a place for the unique capabilities of a fully developed HTS digital technology.

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Multilayer HTS SFQ Analog-to-Digital Converters

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Abstract—**We have fabricated and measured high T_c superconductor single flux quantum 1-bit flux-counting analog-to-digital converters (ADCs). The ADCs were made with a multilayer all-epitaxial process which incorporates 10 edge SNS (superconductor-normal-superconductor) or step-edge grain boundary (SEGB) Josephson junctions with a $YBa_2Cu_3O_{7-\delta}$ groundplane. The ADC consists of a quantizer connected to a Toggle flip-flop through a buffer-like stage. Direct readout of the flux state of the T flip-flop was made with a Read SQUID inductively coupled through a hole in the groundplane. The circuits were operated at 65 K and low speeds. The SNS circuits outperformed the SEGB circuits because of their higher readout voltages and tighter critical current spreads.**

I. Introduction

There have been a number of recent demonstrations of high T_c superconductor (HTS) digital circuits, both single flux quantum (SFQ) architecture [1]-[5] and others [6], [7]. Typically, they have been constrained to the use of a single HTS layer [1]-[5], low operating temperatures [1], [3], [4], or low ultimate operating speed (compared to SFQ logic) [6], [7]. A single-layer circuit process imposes severe topological constraints on circuit layout and low operating temperatures obviate the advantages of HTS materials. In order for an HTS circuit process to reach even the modest integration densities necessary for simple applications, it must include an HTS groundplane with at *least* two additional HTS layers (with the attendant dielectrics) to keep inductances low and for flexibility in interconnection and fan-out/fan-in. One also needs a robust junction technology which allows I_c targeting and the capability of orienting the junction in any direction, if HTS circuits are to become anything more than a laboratory curiosity.

We have fabricated and tested simple HTS flux-counting analog-to-digital converters (ADCs) with an integrated HTS groundplane, using both edge superconductor-normal metal-superconductor (SNS) and step-edge grain boundary (SEGB) Josephson junctions. We chose to build a flux-counting ADC because it contains key elements common to general SFQ circuits. More sophisticated multi-bit flux-counting ADCs have been demonstrated using low T_c superconductors [8]-[12]. Ours is the first demonstration of a multilayer process that is suitable for manufacturing large, high-speed circuits which operate near the temperature of liquid nitrogen.

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II. Design and Fabrication

Our circuit diagram is shown at the top of Fig. 1. It is the first stage (1-bit) of a unidirectional flux-counting SFQ ADC [13], [14], incorporating an asynchronous DC-to-SFQ converter [15] as the quantizer (L1, J1, J2) and a Toggle flip-flop [15] as the bit scaler (J5, J6, J7, J8, L6). Direct readout of the flux state of the T flip-flop is through an inductively-coupled Read SQUID (M1, J9, J10, L7) biased in the voltage

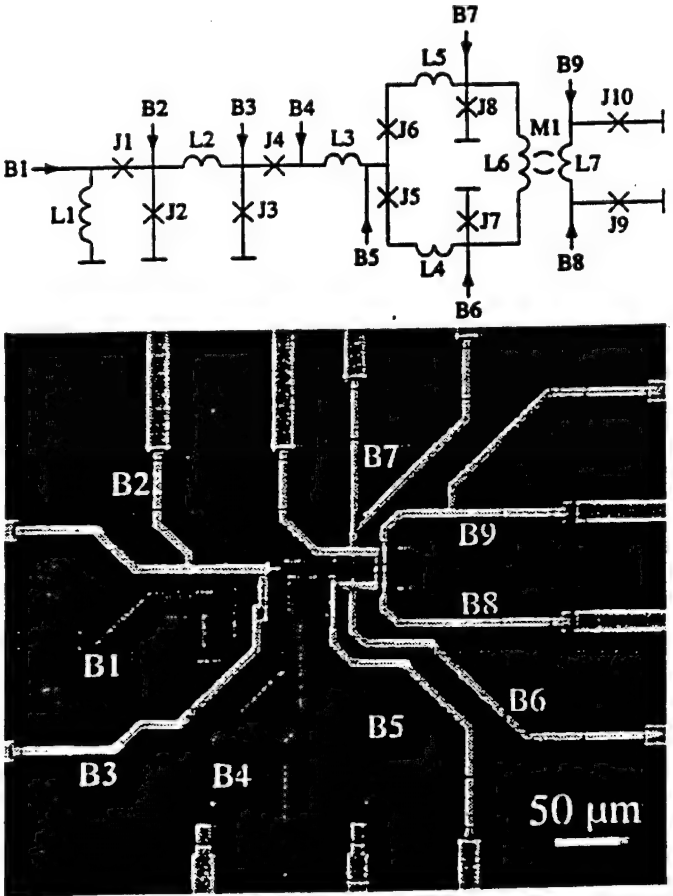

Fig. 1. The one-bit edge SNS ADC. Top: schematic diagram, omitting parasitic inductances and voltage taps: J1 = J2 = J5 = J6 = 2.2 μm wide (nominally 250 μA). J3 = J4 = J7 = J8 = 3 μm (330 μA). J9 = J10 = 1.5 μm (175 μA). L1 = 14.5□, L2 = 4□, L3 = 6□, L4 = L5 = 2□, L6 = 8□ + 6.5 pH, L7 = 3.6□ + 6.5 pH, and M1 = 3.5 pH. B2 = 175 μA, B4 = 120 μA, B5 = 500 μA, B6 = 270 μA, and B7 = −55 μA. Bottom: large scale optical micrograph of the circuit in the edge SNS process. The holes in the groundplane are RF chokes. The base electrode is dark, the counter electrode (with *in situ* Au cap layer) is light. The ground contact vias are not visible on the base electrode islands.

state. It should be noted that J4 is necessitated by the layout constraints imposed by edge-type junctions: there must be an even number of junctions in any superconducting loop.

We made this 10 junction circuit using two HTS multilayer processes (with minor modifications of the design) which are described in detail elsewhere [16]-[19]. We recently developed a 6 layer edge SNS junction process with an integrated groundplane which had both higher I_cR_n and better J_c reproducibility than the SEGB circuit process [17]. The SNS process began by depositing a 225 nm $YBa_2Cu_3O_{7-\delta}$ (YBCO) groundplane onto a $NdGaO_3$ (NGO) substrate. The groundplane was then patterned by photolithography and ion milling. The chips were rotated during all sputter deposition and ion milling steps. All edge angles were kept shallow (~ 25°) to avoid grain boundary formation. A 240 nm thick layer of $SrTiO_3$ (STO) was then deposited and vias were milled. The base electrode (225 nm) and its STO insulator (150 nm) were deposited and patterned together. Finally, the 7% Co-doped YBCO N layer (typically 10-30 nm), the 200 nm counter electrode, and an *in situ* 100 nm Au cap were deposited and patterned. A schematic cross-section of the completed process

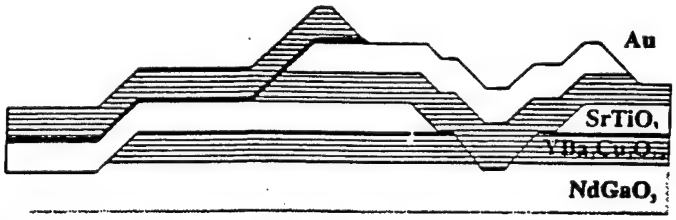

Fig. 2. Schematic of the edge SNS "double via" process. Contact to ground is made through the base electrode. All films were sputter deposited and patterned by ion milling [17]-[19].

is shown in Fig. 2.

SNS junction widths were nominally 1.5, 2.2, or 3.0 μm. The circuit was laid out assuming the critical current density J_c = 500 μA/μm2 (I_c = 175, 250, or 330 μA) and the microstrip inductance per square $L_\square$ = 1 pH at T = 65 K. The Read SQUID was magnetically coupled to the T flip-flop using a hole in the groundplane over which L6 and L7 crossed. This is shown in Fig. 3. The hole was 10 μm long and 19 μm wide and the inductors were 5 μm wide. We approximated this structure as a coplanar waveguide directional coupler to calculate its contribution to the mutual and self-inductances [20]. We calculated the mutual and self inductances for this configuration to be 3.5 pH and 6.5 pH respectively. These estimates are lower bounds on the inductance contribution of the groundplane hole—they neglect the kinetic inductance, but include Chang's empirical end correction [20]. Nominal SNS circuit parameters are given in Fig. 1.

The first ADCs that we successfully fabricated used a 3 layer process which incorporated SEGB Josephson junctions over a groundplane [16]. The general processing parameters and circuit design bore many similarities to the later SNS

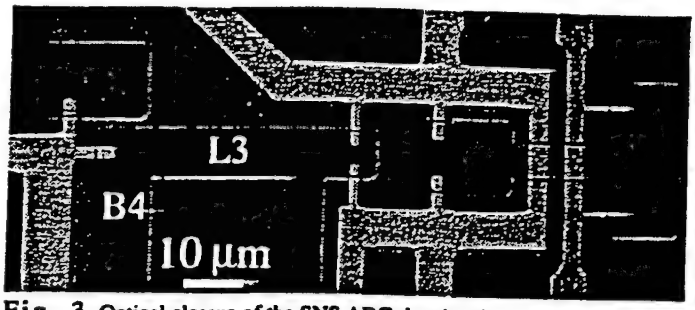

Fig. 3. Optical closeup of the SNS ADC showing the coupled T flip-flop and Read SQUID on the right. Ground contact vias are barely visible as light patches on the base electrode islands. Note the relatively high parasitic inductance (number of squares) necessary to form the junctions.

process discussed above. The SEGB design assumed I_c of the junctions and $L_\square$ to be the same as the SNS process. The groundplane hole coupling was also identical to the earlier scheme. Fig. 4 is an optical micrograph of the area around the T flip-flop and Read SQUID for the SEGB ADC.

JSPICE simulations using the design values for the SNS and SEGB ADCs gave similar values for optimal biases and bias margins [21], [22]. The most sensitive biases were those to the T flip-flop: B5 had the narrowest margins at $2I_{c5}$ ±15%; the biases and margins for the total bias I_T = B6 + B7 and the flux bias I_F = B6 — B7 were $0.4I_{c7}$ ±30% and $0.6I_{c7}$ ±40% respectively (see Fig. 1).

III. Testing and Results

We tested the ADC circuits in a magnetically-shielded, temperature-controlled cryostat which operated above the helium bath. The operating temperature was adjusted using a LakeShore DRC-91C controller so that J_c and $L_\square$ were close to the design values. Biases were supplied by 15-bit digital-to-analog converters (HP 34524/HP 3235). We switched between voltage taps using a relay multiplexer (HP 44470A/HP 3488A). The voltages were measured by a Stanford Research 560 preamplifier and a National Instruments 16-bit ADC board. The lines to the sample were heavily-filtered twisted pairs, with low-pass cutoff frequencies $(RC)^{-1} \approx 10$ Hz.

The edge SNS ADC outperformed the SEGB ADC: it had fewer errors and higher output voltages. This is a reflection of the better J_c reproducibility and higher I_cR_n of the SNS proc-

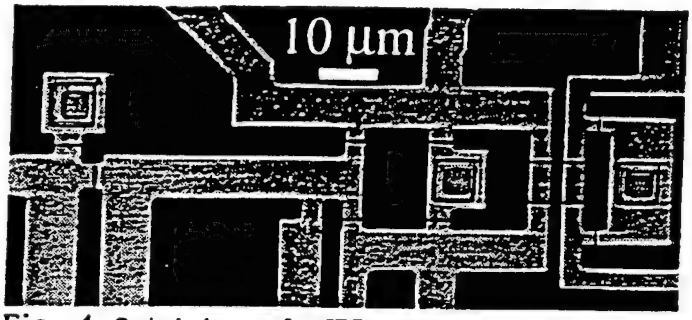

Fig. 4. Optical closeup of a SEGB ADC. Ground contact vias are clearly visible as nested squares. Design parameters were essentially the same as the SNS ADC.

ess. SQUID voltages scale with I_cR_n [23]. We have seen voltage modulations as large as 130 μV in an SNS SQUID (I_cR_n ~ 500 μV) at 65 K [17], which is almost a factor of 10 better than its SEGB counterpart (I_cR_n ~ 50 μV) [16]. Circuit margins are degraded from their ideal values by wide process spreads. The SNS process has produced chips with 1-σ J_c spreads as small as 12% [17], which is much better than we have ever achieved with SEGB junctions. We will therefore concentrate on the characterization of the SNS ADC.

A. Edge SNS ADC

We checked the YBCO film quality by measuring individual SQUIDs on the same chip as the ADC. Microstrip inductances $L_\square$ = 1 pH were measured at 65 K, in agreement with earlier results and design values [16], [17]. We also measured critical currents at a number of points in the circuit. The inferred local J_c = 675-1000 μA/μm² at 65 K was considerably higher than the 500 μA/μm² design value. We could not simply operate the ADC at a higher temperature because of the consequent increase of $L_\square$. The fabricated circuit suffered from parasitic inductances associated with the narrowness of the junctions and the layout of the ground contacts, which amounted to 1-2 □ per junction (see Fig. 3). Additionally, we find that our estimate for the self inductance contribution of a groundplane hole (which neglected the kinetic inductance) was too low.

In Fig. 5 we plot the modulation of the Read SQUID I_c vs. the control current I_{con} = (B8 — B9)/2. The depth of modulation of I_c yields the total inductance of the SQUID, assuming no asymmetry between junctions [17]. However, the effective total inductance inferred from the modulation depth (45 pH) is much larger than the sum of the geometric and groundplane hole inductance (~ 20 pH). This implies a significant asymmetry between J9 and J10 [23]. Additionally, the critical currents of the 1.5 μm (nominally 175 μA) junctions (J9 and J10) were often low—we suspect the culprit was ion milling edge damage. The periodicity of I_c gives us the microstrip inductance between current contacts [16], [17]. (See Fig. 3 for the Read SQUID geometry.) At 65 K, L7 = 13.1 pH, of which ~ 4 pH are due to microstrip. The inductance due to the groundplane hole is therefore ~ 9 pH, almost 40% higher than our design estimate of 6.5 pH. However, the measured mutual inductance between L6 and L7 was 3.3 pH, quite close to our estimate of 3.5 pH. As a consequence of the high J_c and additional sources of inductance, the LI_c products were as much as a factor of 2 higher than the design values in Fig. 1.

Testing of the ADC was relatively straightforward. Ramping up the current B1 causes J2 to pulse every = Φ_0/L1, with the position of the first threshold set by the bias B2. If the rest of the circuit is properly biased, these pulses propagate to the bistable T flip-flop and trigger it to switch states. The flux state of the T flip-flop (i.e., the current in L6) can be directly sensed by the Read SQUID, which is biased into

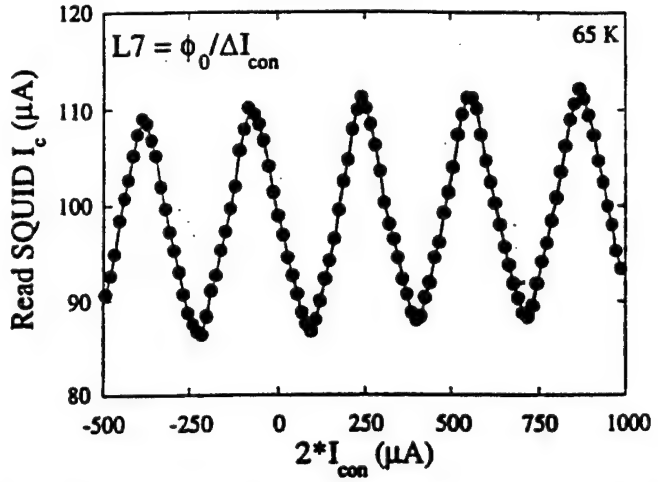

Fig. 5. I_c vs. $2I_{con}$ = B8 — B9 for the Read SQUID. The period of ~ 315 μA gives a value for L7 = 13.1 pH, ~ 9 pH of which is due to the hole in the groundplane. The depth of modulation implies a total SQUID inductance of ~ 45 pH, which is much greater than the geometric inductance. Asymmetry between junctions J9 and J10 is the source of this discrepancy.

the voltage state. As the flux in L6 toggles between 0 and Φ_0, the Read SQUID voltage should change between two corresponding levels.

Our usual procedure was to set the DC biases to their nominal levels (scaled by the "local" J_c) and then fix an appropriate bias point for the Read SQUID. We then ramped B1 at ~ 15 μA/s to 0.5-2 mA while watching the voltage across the Read. Biases B5-7 were then adjusted to achieve proper operation. Alternatively, we determined bias points for the T flip-flop by measuring its lobe boundaries. The lobe boundary measurements were difficult to interpret because the inductances were often large enough to store multiple flux quanta.

In Fig. 6 we plot two successive traces of the Read SQUID voltage V against B1, the input current to the quantizer, at 65 K. We averaged the voltage for ~ 100 ms at each

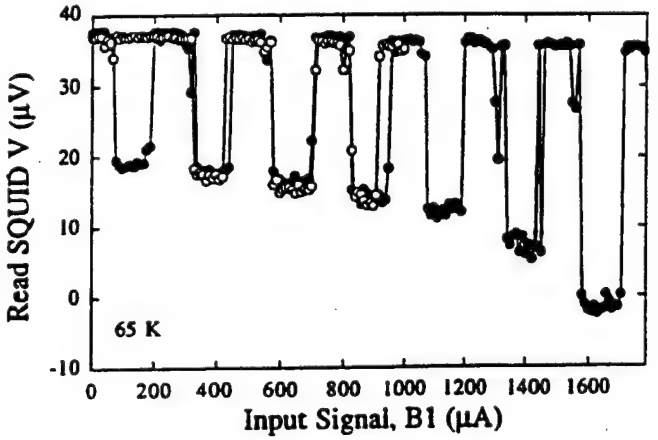

Fig. 6. The SNS ADC in operation at 65 K. The Read SQUID voltage switches between two levels, corresponding to the flux state of the toggle flip-flop. The open and closed symbols are two successive ramps of B1 taken two minutes apart which show some instability in the switching thresholds. However, the 125 μA average period agrees well with the design value, Φ_0/L1 ≈ 130 μA.

bias point. Occasionally, a switch occurred during averaging. This shows up in Fig. 6 as an intermediate voltage between the two "stable" values. The Read voltage has a ≈ 125 μA period. The microstrip inductance inferred from this period $L_{\square} = (\Phi_0/\Delta I)/14.5\square = 1.1$ pH agrees well with our recent independent measurements [16]-[19]. The drift in the Read voltage is an artifact of the measurements. This particular sample had ground contact problems: due to a resistive ground contact, large input signals modified the Read SQUID bias, changing its output.

Both traces show evidence for threshold instability. Our ADC is not immune to thermal and electronic noise: first, variations in J_c decrease the operating margins of the circuit; the closer circuit operation is to the margins, the higher the error rate. Second, it is not clear that the design values of I_c (J7 = J8 = 330 μA) themselves are large enough at 65 K to ensure a low thermal-activation error rate [4]. Our measurements of J_c on this circuit showed a wider spread (675-1000 $\mu A/\mu m^2$) than the best we have obtained for the edge SNS process [17]. Both vulnerabilities are reflecued in our measurements of the margins of B5, I_F, and I_T, which were all smaller than 5%. Admittedly, the margins are ill-defined, since even in the best case, errors were present.

IV. Conclusions

We have designed, fabricated, and demonstrated HTS SFQ 1-bit counting ADCs which operated at low speeds at 65 K. We used a 6 epilayer process which included an integrated groundplane and edge SNS junctions as well as a 3 epilayer SEGB process. This is the first demonstration of a circuit process extendible to making SFQ circuits of technological interest (10s-100s of Josephson junctions) which operate at high temperatures.

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Inductance measurements in multilevel high T_c step-edge grain boundary SQUIDS

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Multilevel high T_c SQUIDs, suitable for digital circuit applications, have been fabricated and tested. The devices employ a $YBa_2Cu_3O_{7-\delta}$ (YBCO) ground plane, an epitaxial $SrTiO_3$ insulator, and a YBCO microstrip layer. Junctions are formed by the step-edge grain boundary process, with a ground plane contact for the "low" side of each junction, using only isotropic sputtering and milling techniques. Control current is directly injected in a microstrip segment of the SQUID loop, allowing us to measure the microstrip inductance, and thus to infer the magnetic penetration depth of the YBCO. The SQUIDs are operational above 77 K, at which temperature we infer a penetration depth of 350 nm. The temperature dependence of the penetration depth is found to be in reasonable agreement with the Gorter–Casimir form close to T_c. © *1994 American Institute of Physics.*

The development of a high-temperature superconducting (HTS) digital circuit process requires the development of reproducible Josephson junctions, and the integration of these junctions into an epitaxial, multilayer process. Such layers would include superconductors, epitaxial insulators, and probably epitaxial resistors. Of particular importance is the use of a superconducting ground plane, to keep circuit inductances values both low and well defined.

Low inductances are essential for single flux quantum circuits, so that a single quantized voltage pulse, $\Phi_0=h/2e=1000$ pH μA, can generate sufficient current in a load inductor. Even simple structures, like Josephson digital transmission lines for logic gate interconnections, will need inductors as small as 5 pH between junctions.

Single flux quantum circuits can obtain logic clock speeds above 10 GHz with junction $I_cR_n=100$ μV. In contrast, circuits built without ground planes will have large interconnection inductances, requiring voltage-state logic gates, and are unlikely to operate at GHz clock rates.

Here, we report the first demonstration of multilayer high-temperature superconducting SQUIDs, suitable for digital circuit applications in the 65- to 77-K temperature range. Further, our process employs isotropic film deposition and etching techniques, with no favored direction for the junctions, and thus is potentially extendible to complex circuits.

A previous report by Missert *et al.* described the fabrication of step-edge superconductor-normal-superconductor (SNS) junctions over a ground plane, using directional deposition of the YBCO to ensure a discontinuity in the YBCO over a step in a deposited insulator, with a noble metal deposited as the normal barrier.[1] These devices operated as SQUIDs only up to 20 K, preventing the measurement of inductance as a function of temperature up to the more useful 65- to 77-K temperature range.

We have fabricated step-edge grain boundary junctions over a YBCO ground plane, using a process which is designed from the outset to allow junctions to be fabricated in four directions, for flexibility in circuit layout. Since the fabricated devices operate to above 77 K, we have measured the inductance of a microstrip portion of the SQUID loop as a function of temperature, and have inferred the temperature-dependent magnetic penetration depth for our YBCO films.

Our fabrication process uses off-axis rf magnetron sputtering for both YBCO and $SrTiO_3$ films, with YBCO sputtered in oxygen, argon, and water,[2] and $SrTiO_3$ in oxygen and argon. Typical deposition temperatures were in the 670–700 °C range for both materials. Substrates rotated during deposition to ensure uniformity and edge coverage. Patterning of each layer was by argon ion milling with a 20-cm diam rf ion source, with beam energies of 150 and 300 eV for the YBCO and $SrTiO_3$, respectively. Samples were clamped to a water-cooled, rotating sample table during milling. The choice of a higher voltage for the $SrTiO_3$ is dictated by the need for a well-collimated beam for etching of sharp steps in this layer, while the slightly more divergent beam obtained at 150 eV is more suitable for milling tapered edges in the YBCO layers. An end-point detector based on secondary ion mass spectroscopy was used to determine when to terminate each etch step.

A YBCO (001) ground plane, typically 200 nm thick, was deposited first on a single-crystal substrate of $NdGaO_3$(110) or $LaAlO_3$(001) (cubic crystal approximation), and its pattern defined with photoresist, with a process designed to give tapered photoresist sidewalls. The film was etched by ion milling at a shallow angle, which, in combination with the tapered resist, ensured that the edges of the YBCO should be tapered to ensure good contact with the second YBCO layer and good coverage by the $SrTiO_3$. After ion milling the photoresist was stripped using a combination of rf oxygen plasma, and soaking in acetone. We have found from XPS observation that this process leaves the surface of the YBCO relatively free of both hydrocarbons and carbonates.

After deposition of a 200-nm $SrTiO_3$ layer, another photoresist process, this one designed to produce a steep resist profile, was used to define its pattern. Ion milling at close to normal incidence was then used to etch the $SrTiO_3$ film, producing sidewalls with angles thought to be between 0° and 20° from vertical, based on the observation of test samples, viewed in cross section in a scanning electron microscope (SEM). After the resist clean-up a second 200-nm

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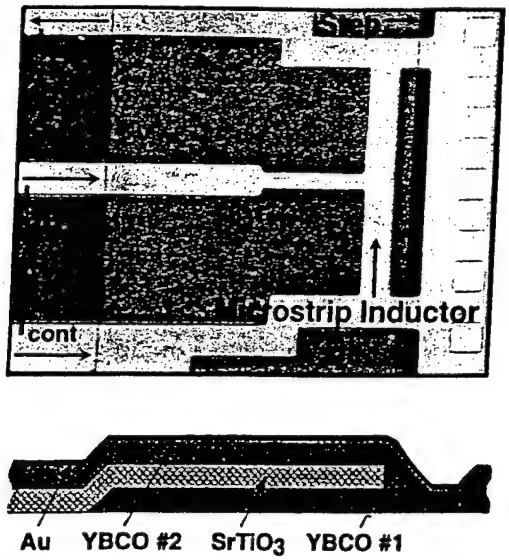

FIG. 1. Micrograph of a fabricated multilayer HTS SQUID, and schematic cross-sectional view. The microstrip inductor is 10 μm wide.

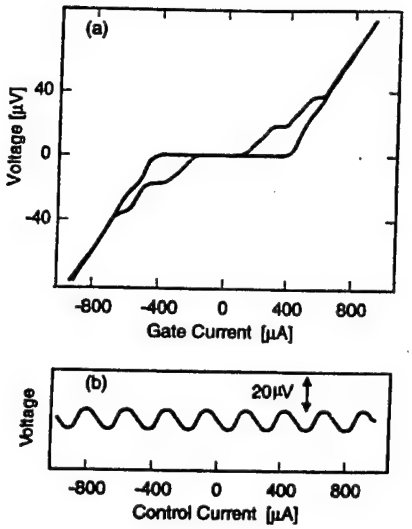

FIG. 2. Current-voltage characteristic, with and without 10-GHz radiation (a), and voltage vs control current, (b), for a SQUID with a 50-μm-long microstrip inductor. Both are at 70 K.

layer of YBCO was deposited, followed by approximately 30 nm of Au, *in situ*. This bilayer was then patterned by photolithography and ion milling, with no particular precautions taken in defining the profile of the etched material for this last layer. The Au was left in place both to provide low resistance contacts and to protect the grain boundary junctions from processing damage, which we have observed in "uncovered" junctions.

It is worth noting that we have not found it necessary to use a deposited milling mask, such as Nb[3,4] or diamondlike carbon,[5] to produce sharp steps in our deposited $SrTiO_3$, a significant process simplification. This is also in contrast to our own work in making junctions on a step etched into a single-crystal $NdGaO_3$ substrate, where a metal mask was required to obtain sharp steps. This is an example of the often significant differences in the etching properties of the various materials being employed in HTS process development.

Figure 1 shows a photograph and a schematic cross-sectional view of a fabricated SQUID. The SQUIDs incorporate microstrip inductors, L_μ, of 10-μm width and various lengths, into which a control current, I_{cont} can be directly injected to provide a flux, $\Phi = L_\mu I_{cont}$. The junctions, of width 6 or 10 μm, contact the ground plane in a region that contains a grid of holes, seen on the right in Fig. 1, which allow both c-axis and $a-b$-axis contact between the two YBCO layers.

In exploring the processing parameters involved in fabricating these devices we have produced ten chips, with six SQUIDs on each. The quality of the devices, as measured by, for example, amplitude of voltage modulation, varied with the detailed process parameters, which are still being optimized, but the overall yield of modulating SQUIDs was about 70%. Failures of many of the remaining 30% can be traced to observable defects in the fabrication process.

The current-voltage characteristic of a typical SQUID at 70 K is shown in Fig. 2(a), with and without 10-GHz radiation, and exhibits behavior generally consistent with the resistively shuned junction model, with the expected downward curvature. Most devices show evidence for weak constant-voltage steps in the I-V characteristic in the absence of microwaves, which we have not seen in junctions fabricated directly on $NdGaO_3$ and $LaAlO_3$ substrates, without a ground plane. This may be due to L-C resonances associated with the high dielectric constant of the $SrTiO_3$.

Figure 2(b) shows SQUID voltage versus control current, at 70 K. The period of this modulation is determined by the inductance of the microstrip portion of the loop, L_μ including any parasitic inductance associated with the center tap and the ends, through

$$\Delta I_{cont} = \frac{\Phi_0}{L_\mu}, \tag{1}$$

where Φ_0 is the superconducting flux quantum. By measuring this period, directly from oscilloscope traces, as a function of temperature we determine the inductance as a function of temperature. This is shown in Fig. 3(a) for a 50-μm-long, 10-μm-wide microstrip inductor.

To infer an effective penetration depth, λ, for our YBCO films we assume that the two films are identical, and use the following expression for the inductance per square of a superconducting strip over an infinite ground plane:[6]

$$L = \frac{\mu_0 d \kappa}{w}\left[1 + \frac{2\lambda}{d}\coth\left(\frac{b}{\lambda}\right)\right], \tag{2}$$

where, d is the insulator thickness, w the microstrip width, b the superconductor thickness, and κ is a factor that determines the field strength at the center of the finite width microstrip. Here, λ is for transport current and magnetic field (neglecting small fringing fields) parallel to the $a-b$ plane, and thus is λ_{ab} of Ref. 7. The value of κ for our microstrip can be determined to be approximately 0.93 from Fig. 3.09d of Ref. 6, using our experimental values of $d = 200$ nm and $w = 10$ μm. Combining this with the experimental value, $b = 220$ nm, and measured values of L_μ for the 50-μm-long

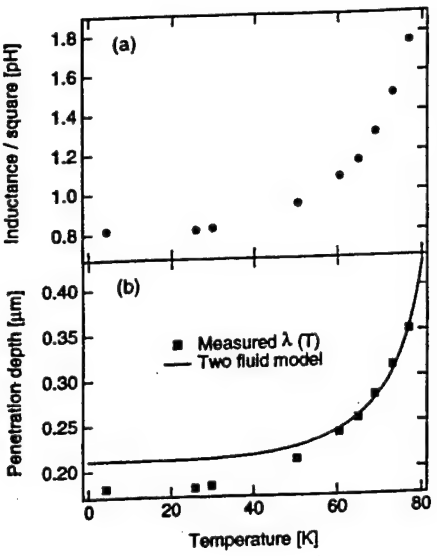

FIG. 3. (a) Measured inductance per square, in picohenries for a SQUID with a 50-μm-long microstrip inductor. (b) Penetration depth of our YBCO films, inferred from the measured inductance. The solid line is a fit to the data above 60 K using the Gorter–Casimir form for the temperature dependence of the penetration depth: $\lambda(T)=\lambda_0/[1-(T/T_c)^4]^{1/2}$.

microstrip of Fig. 3(a), we solve Eq. (2) to determine λ. The result is shown in Fig. 3(b) as a function of temperature. The magnitude of the inferred penetration depth is in good agreement with measurements by other techniques.[7] The solid line in Fig. 3(b) is a fit to the Gorter–Casimir form for the temperature dependence of the penetration depth: $\lambda(T)=\lambda_0/[1-(T/T_c)^4]^{1/2}$, for the data above 60 using the measured zero-resistance transition temperature of 86 K.

In summary, we have fabricated HTS step-edge grain boundary SQUIDs incorporating a HTS ground plane, using a process which allows junctions to face in all four directions. These SQUIDs have critical currents of a magnitude useful for digital circuit operation in the 65- to 77-K temperature range, and exhibit good Josephson behavior. Measurements of the inductance of the microstrip portion of the SQUID loop have allowed us to infer a penetration depth for our YBCO films, whose magnitude and temperature dependence are consistent with other measurements, and with the requirements of low-inductance interconnects in digital circuits. Further work is required to determine the reproducibility of the process, especially that of junction critical current, and to replace the $SrTiO_3$ with a lower loss insulator.

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High-T_c superconductor/normal-metal/superconductor edge junctions and SQUIDs with integrated groundplanes

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Epitaxial, high-T_c superconductor/normal-metal/superconductor (SNS) edge-geometry weak links and superconducting quantum interference devices (SQUIDs) have been fabricated with integrated $YBa_2Cu_3O_7$ (YBCO) groundplanes and $SrTiO_3$ insulators, using a process which incorporates six epitaxial layers. The SNS edge junctions were produced using off-axis sputtered films and Co-doped-YBCO normal metal interlayers. These devices show excellent performance with typical critical current-resistance (I_cR_n) products of 500–800 μV for 100–150 Å thick normal metal layers at 65 K, and 1-σ critical current density (J_c) spreads as small as 12%. SNS SQUIDs incorporating groundplanes exhibit voltage modulation of up to 130 μV at 65 K and 40 μV at 77 K. SQUID inductance measurements indicate microstrip inductance values of 1 pH per square at 65 K.
 [S0003-6951(96)00925-4]

Single flux quantum (SFQ) digital circuits based on high-temperature superconductors (HTS) have the potential to perform logic operations at 10 GHz clock rates while dissipating only a microwatt per gate. In order to fully realize this potential, it is necessary to develop a circuit process which integrates reproducible Josephson junctions into epitaxial multilayers. In particular, a superconducting groundplane is required to keep circuit inductances low enough that a single quantized voltage pulse can generate sufficient current in a load inductor.

We have previously reported the incorporation of YBCO-based step-edge grain boundary junctions with a HTS groundplane, demonstrating multilayer SQUIDs with microstrip inductances as low as 1 pH per square at 65 K.[1] The practicality of such junctions for large-scale circuits was, however, limited by their I_cR_n values (typically 50–100 μV at 65 K) and poor critical current uniformity (typically no better than 30%, 1-σ, on chip).

Here we report the demonstration of superior SNS edge junctions, integrated with a groundplane, in a process incorporating six epitaxial layers. These junctions exhibit I_cR_n values of 500–800 μV at 65 K, and critical current uniformities as low as 12% (1-σ), making them more promising candidates for a manufacturable HTS digital circuit process. Along with results reported by Conductus,[2] these are the first SNS edge junctions with separate but integrated HTS groundplanes,[3] which operate above 50 K.[4]

The YBCO, Co-doped-YBCO, and $SrTiO_3$ (STO) films used in this work were deposited by off-axis rf magnetron sputtering following processes detailed elsewhere.[5] An essential condition for circuit-compatible YBCO growth is the production of smooth, outgrowth-free films, which helps ensure good electrical isolation between successive YBCO layers. In practice it is found that smooth YBCO film growth by off-axis sputtering is sensitive to deposition system cleanliness, as well as surface cleanliness of the underlying epilayer. In our process, each epitaxial growth step over a patterned underlayer was preceeded by *ex situ* oxygen plasma and 150 eV Ar/O_2 ion mill cleaning steps. We also optimized insulator growth temperatures to enable proper oxidation of the buried groundplane, while maintaining an adequate epitaxial template for growth of high quality overlayers.[6] Acceptable STO growth temperatures were in the range of 670–690 °C, compared to typical YBCO deposition temperatures of 720–730 °C. The normal metal layers were $YBa_2Cu_{2.79}Co_{0.21}O_{7-\delta}$ (7% Co-doped YBCO), optimized for smoothness and maximum Co incorporation (minimum T_c). Typical T_c values for Co–YBCO layers were 51–58 K.

Our multilayer device structure, shown in cross section in Fig. 1, is based on SNS edge-geometry weak links fabricated over a YBCO groundplane. We chose the buried groundplane geometry to minimize the processing steps needed to complete the SNS device after the counterelectrode deposition, although there is no *a priori* reason to rule out the use of groundplanes on top. The choice of YBCO SNS edge junctions was driven by the known advantages of this technology,[7,8] and by the promising device results that have been achieved using SNS edge junctions with Co-doped-YBCO normal metal layers.[9,10]

The process used to pattern each layer except the counterelectrode was designed to produce an edge taper of 20°–30° from the horizontal, independent of edge orientation. This was achieved by using Hoechst 1518 resist, reflowed

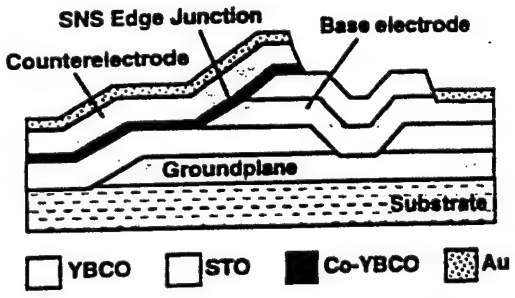

FIG. 1. Schematic cross section of an YBCO/Co-YBCO/YBCO SNS edge junction integrated with an epitaxial YBCO groundplane. The multilayer structure includes six epitaxial layers and contact vias to the groundplane and base electrode.

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after patterning for 5 min at 130 °C, and then Ar ion milling the rotating substrate at 150 eV and 50° from normal. Each patterning step was followed by the cleaning process described above. The fabrication began with the deposition of a *c*-axis-oriented 2250 Å YBCO groundplane on a (110) $NdGaO_3$ substrate, followed by growth of a STO passivation layer. The groundplane was patterned, a 2400 Å STO layer was deposited, and via holes to the groundplane were defined. Next, an 1100–3500 Å YBCO base electrode and 1500 Å STO capping layer were grown and patterned. After an *in situ* Ar ion mill clean we deposited 100–250 Å of epitaxial Co-doped YBCO, followed by growth of the YBCO counterelectrode, an *in situ* anneal, and finally *in situ* sputtering of a gold contact layer near room temperature. Via holes were patterned down to the base electrode, and gold was sputtered and lifted off in the vias to provide base electrode contacts. Finally, the YBCO counterelectrodes were defined with a straight-wall resist process and Ar ion milling.

Our standard test pattern consisted of 20 junctions arrayed on four sides of a square base electrode with nominal widths of 2, 4, and 6 μm, and 75×75 μm^2 groundplane patches under half the junctions. The layout had four or nine subchips on each 1-cm^2 chip, and the subchip to be tested was wire bonded into a 44 pin carrier. Subchip designs included junction test structures, SQUIDs, and SFQ circuits. Automated chip testing was done in a temperature controlled, magnetically shielded cryostat with three orthogonal pairs of magnetic field coils.

The $I-V$ characteristics on a typical chip for the four 4-μm-wide SNS junctions over groundplane patches are shown in Fig. 2. The data were taken at 65 K on devices with 150 Å Co-doped-YBCO normal metal interlayers. The average device parameters for these junctions are: $J_c = 1.27 \times 10^5$ A/cm^2 with a 1-σ spread of 20%; $I_cR_n = 587$ μV with a 1-σ spread of 15%; and $R_nA = 4.8 \times 10^{-9}$ Ω cm^2 with a 1-σ spread of 24%. A key point to note is that these junction parameters are essentially identical to those for junctions without groundplanes: fabricating the edge junctions above the patterned groundplane and groundplane insulator did not degrade the device quality. Isolation between the junction film layers and the groundplane was checked on test structures located adjacent to the actual junctions. Room-temperature measurements verified typical isolation resistivities greater than 10^6 Ω cm. Studies of via test structures and circuits located on the junction chips demonstrated base-electrode-to-groundplane vias with critical currents greater than 9 mA, the current limit of the test setup.

Another important issue is that these SNS weak links have large I_cR_n and R_nA products relative to most reported SNS device results. For Co-doped YBCO thicknesses of 100–150 Å, the I_cR_n products are typically in the range of 500–800 μV at 65 K, and 150–250 μV at 77 K, values which are more than adequate for production of SFQ circuits. The R_nA products are ~5–10 times larger than expected from the Co-doped YBCO resistivity and layer thicknesses. We believe the relatively high junction resistances are due to inhomogeneous S–N interface resistances. Nonuniform conduction through a SNS device can reduce the active area and increase R_n without reducing I_cR_n, if highly conducting regions are separated by nonconducting

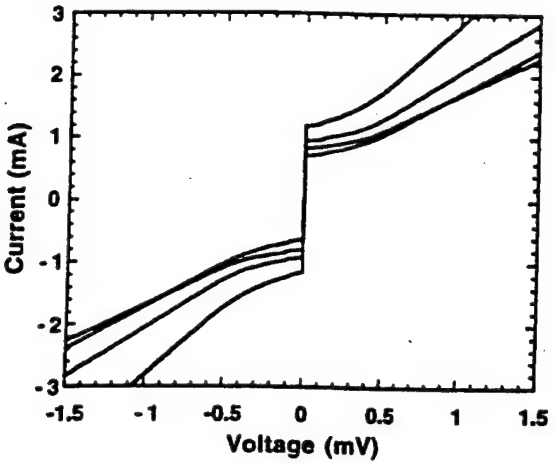

FIG. 2. Current–voltage characteristics at 65 K for the four 4-μm-wide SNS junctions with integrated groundplanes on a typical test chip. The Co-doped YBCO thickness is 150 Å and the average I_cR_n product is 587 μV.

areas.[11,12] We find, in fact, that the R_nA products vary as a function of the base electrode edge formation process, suggesting that the base electrode–normal metal interface contributes directly to the high observed resistances. Inhomogeneous conduction through this interface could result from nonuniform edge damage or a patchy insulator layer caused by sputtering the insulator overlayer down onto the base electrode edge. Although the origin of the large R_nA products is not fully understood, we have demonstrated reproducible control of device resistances, and the high resistances we obtain are important for many applications.

The 1-σ critical current variations we observed ranged from 12% to over 40% on the eleven 1-cm^2 chips (16 subchips) we have tested with groundplanes. In most cases, the 1-σ spreads for the devices over groundplanes were comparable to companion junctions without groundplanes. Larger I_c spreads were generally associated with rougher base electrode or counterelectrode films. As progress is made in optimizing film growth for smooth surface morphology we expect to routinely achieve the 10%–15% I_c spreads required for small-scale SFQ circuits (<1000 junctions).

Shielding of the groundplanes was qualitatively verified by magnetic-field I_c modulation studies. Figure 3 is a plot of I_c versus magnet current for a field perpendicular to the substrate at 77 K for junctions with and without a groundplane patch. Both curves show I_c modulation approximately consistent with the expected $\sin(x)/x$ behavior, indicating good large-scale uniformity of the normal metal layers. However, the junction over the groundplane exhibits a modulation period approximately four times that of the other junction, demonstrating the magnetic shielding effect of the superconducting film. Complete shielding is not observed due to the large demagnetization factor associated with a field applied normal to the groundplane film.

In order to quantitatively characterize the effectiveness of the ground plane, we fabricated direct-injection SQUIDs, similar to those previously fabricated using step-edge grain boundary junctions.[1] The applied control current, I_Φ, flowing through a microstrip portion of the SQUID inductor, is given by $(I_1 - I_2)/2$, where I_1 and I_2 are the current injected

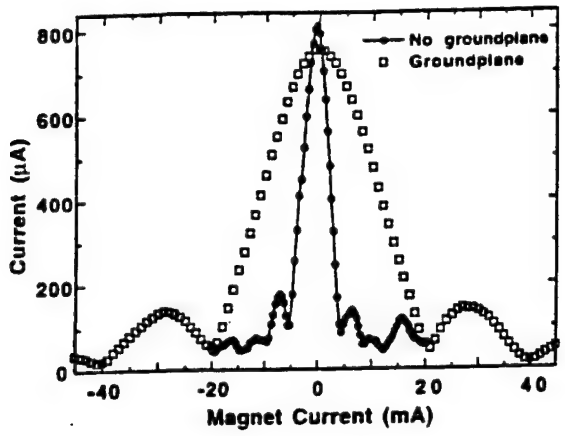

FIG. 3. Plot of critical current vs magnet current for fields normal to the substrate for 4-μm-wide junctions with and without groundplanes at 77 K.

in the left and right ends, respectively, of the inductor. Figure 4(a) shows the SQUID voltage as a function of I_Φ, for various fixed values of the total bias current I_1+I_2. The period, ΔI_Φ, of these modulation curves is related to the inductance of that portion of the SQUID loop, L_μ, by

$$\Delta I_\Phi = \frac{\Phi_0}{L_\mu}, \tag{1}$$

where Φ_0 is the superconducting flux quantum. By measuring this period as a function of temperature we determined $L_\mu(T)$. This is shown, normalized to the inductor length, in Fig. 4(b) for five SQUIDs with varying lengths of microstrip inductor. The inductance per square values obtained are in good agreement with those reported in Ref. 1. Using the expression for the inductance of a strip over an infinite groundplane, as in Ref. 1, we infer an effective penetration depth, for current and field both in the a-b plane, of $\lambda_{a\text{-}b} \approx 0.2$ μm at 65 K, consistent with our previous measurements.

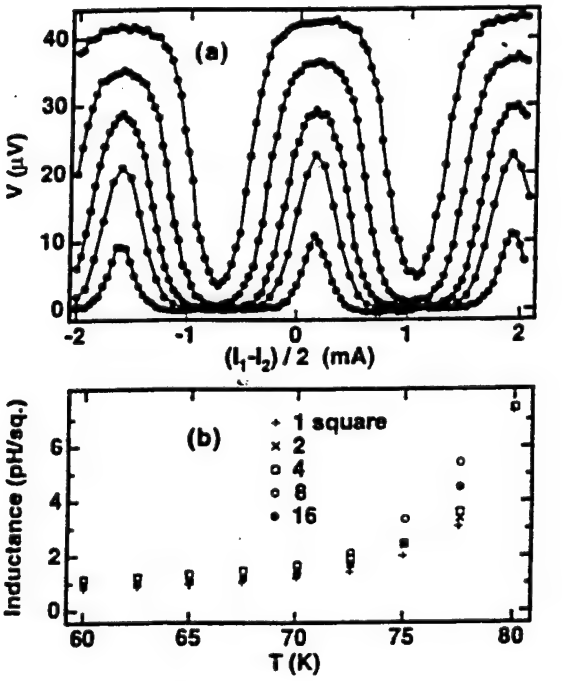

FIG. 4. (a) 77 K voltage modulation as a function of control current for a direct-injection SNS edge junction SQUID with integrated groundplane. The bias currents are 480, 490, 500, 510, and 520 μA. (b) Measured inductance per square for five SQUIDs as a function of temperature.

While the period of the voltage modulation is related to the inductance of the microstrip inductor into which the control current is injected, the *depth* of modulation is related to the *total* inductance of the SQUID. Using standard SQUID models,[13] including the effects of thermal fluctuations,[14] we estimate an upper limit (assuming negligible asymmetry in the junction critical currents) on the total inductance of the smallest SQUID of Fig. 4(b) to be about 12 pH at 65 K. The inductance is thus dominated by the 3 μm wide junction legs of the SQUID, and their contacts to ground. Minimizing this unwanted inductance, especially for our relatively high J_c devices, will require careful layout and junction alignment.

In summary, we have demonstrated high quality SNS edge junctions and SQUIDs integrated with superconducting groundplanes using a circuit-compatible omnidirectional edge formation process. The junctions exhibit I_cR_n products of 500–800 μV at 65 K with 1-σ I_c spreads down to 12%. Effectiveness of the groundplanes was verified by single junction I_c-modulation studies and by direct injection SQUID measurements. The SQUIDs show voltage modulation of up to 130 μV at 65 K and 40 μV at 77 K, and analysis of the SQUID data gives microstrip inductances of ~1 pH/□ at 65 K. These devices are suitable for fabrication of small-scale HTS SFQ circuits and our results in that area will be reported elsewhere.

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Single-Flux-Quantum Circuits Based on YBCO Step-Edge-Grain-Boundary Junctions

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Abstract - A consistent motivation for the investigation of high temperature superconductor (HTS) Josephson junctions has been the desire for high-speed, low-power digital circuits. The fabrication of meaningful single-flux-quantum (SFQ) circuits in HTS technology requires a multilayer process for control of circuit inductances. Previous investigators have reported simple SFQ circuits in a single $Y_1Ba_2Cu_3O_x$ (YBCO) layer process or two junction SQUIDs in a two YBCO layer process. Based on these previous results, we have designed and fabricated simple SFQ circuits using a two YBCO layer process with step-edge-grain-boundary junctions.

I. Introduction

Superconductive digital circuits have been shown to operate at multi-GHz clock rates with orders of magnitude lower power consumption than semiconductor circuits of similar complexity. The extension of this technology to encompass the use of high temperature superconductivity (HTS), coupled with the availability of compact, low-cost cryocoolers, will have an immediate impact on advanced communication, signal processing, and defense electronics systems.

Single-Flux-Quantum (SFQ) logic has advantages over other types of superconducting logic in terms of speed and power [1]. Moreover, SFQ logic uses non-latching Josephson junctions, and thus is compatible with HTS junctions demonstrated to date. This has been demonstrated through SFQ circuits fabricated using a single level $Y_1Ba_2Cu_3O_x$ (YBCO) process[2]. This paper describes the design and fabrication of simple SFQ circuits in a multilevel YBCO technology. The choice of technology was based on the ability to fabricate both Josephson junctions and multilayer HTS films. For practical digital circuits, junctions with critical currents (I_c) ranging from 100 μA to 500 μA, and products of I_c and normal state resistance (R_n) of more than 300 μV are desired.

Approaches to YBCO junction fabrication have met with varying degrees of success. Bi-crystal junctions which require fused substrates have yielded good junction properties, but at high cost and with severe limitations on circuit layouts. Junctions with deposited barriers, such as edge junctions, are difficult to integrate into multilayer structures since they require additional epitaxial film depositions. Step-edge-grain-boundary (SEGB) junctions, which are formed by discontinuities in crystal orientation as the HTS film covers a step in the substrate, have the disadvantage of rather large spreads in I_c, but are more easily integrated with multilayers. For circuits with few junctions, variations from designed critical currents can be compensated by adjusting the dc bias current to each junction.

II. Fabrication

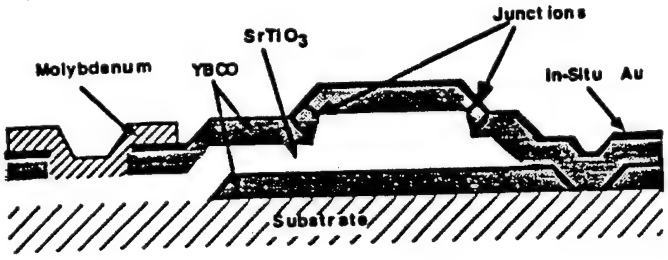

Fig. 1 Cross section of the process used to fabricate single-flux-quantum circuits with step-edge-grain-boundary junctions.

We have fabricated circuits using a five mask level process as illustrated in Fig. 1. This process, which uses two levels of YBCO deposition, is based upon that used by Forrester et al. to fabricate dc SQUIDs [3].

The first deposition of YBCO (2000Å) formed the ground plane. This layer was removed from the region outside the active circuits by ion milling to reduce the possibility of shorting from bias leads to ground and to provide reliable end-point detection for the milling operation.

Following patterning of the ground level YBCO, a 3000-4000 Å layer of $SrTiO_3$ was deposited as a dielectric. This level was patterned twice using two different masks and two different sets of ion-milling conditions. The first etch,

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(1500-2000 Å) was used to define steps for the formation of junctions. This process step was designed to produce a sharp step, with rotation of the substrate during milling allowing junctions of arbitrary orientation. In practice, only orthogonal junctions were used. The second milling step penetrated the dielectric and was designed to produce a much shallower ramp (≤ 30°). This shallow ramp was intended to permit a transition from the microstrip level to the ground plane level without introducing an unwanted junction. By using a two-step dielectric etch we were able to combine floating and grounded junctions, a requirement for SFQ decision circuits, while fabricating all junctions with the same process steps. This, in turn, reduced run-to-run process variations which contribute to non-uniform junction critical currents.

The second level of YBCO formed the inductors and junctions of the SFQ circuits. Junction contacts to ground were made through ground plane vias to provide a- and b-axis contact. Following the active layer YBCO deposition a thin layer of gold was deposited in-situ both to act as a passivation layer and to provide a good contact for wire bonding.

The final process step was deposition of a molybdenum film for 1 ohm per square resistors.

III. Circuit Layout

Circuit layouts were generated for the following circuits: set-reset flip-flop, T-flip-flop (TFF) with digital readout, T-flip-flop with voltage mode readout, SFQ quantizer, one-bit SFQ analog-to-digital converter, and sigma-delta modulator. These circuits are well known [1], [4], [5] and will not be described in detail here. A T-flip-flop will be used as an example to illustrate layout concepts.

Figure 2 shows the circuit diagram and the corresponding mask layout for a SFQ TFF with a magnetically coupled readout SQUID. Junctions in the TFF have designed critical currents of 233 μA for the upper junctions and 333 μA for the lower junctions. Critical currents are scaled by the width of the junction. Individual dc bias leads to each junction were included to allow compensation for variations in junction critical currents. Additional leads were provided for average voltage mode testing.

While, in principle, the process allows junctions in arbitrary orientation, only x and y orientations were used in the present work. The fact that two junctions are formed at each step has been ignored in the circuit layout, under the assumption that one of the junctions will dominate, with the second junction having minor phase variations. This is not inconsistent with the observed behavior of dc SQUIDs fabricated by a similar process [3].

Junction contacts to ground are formed through the edges of ground plane vias, as shown in Fig. 2, to allow a- and b-axis current flow. As noted in the previous section, the shallow ramp of the insulator vias was not expected to result in junctions.

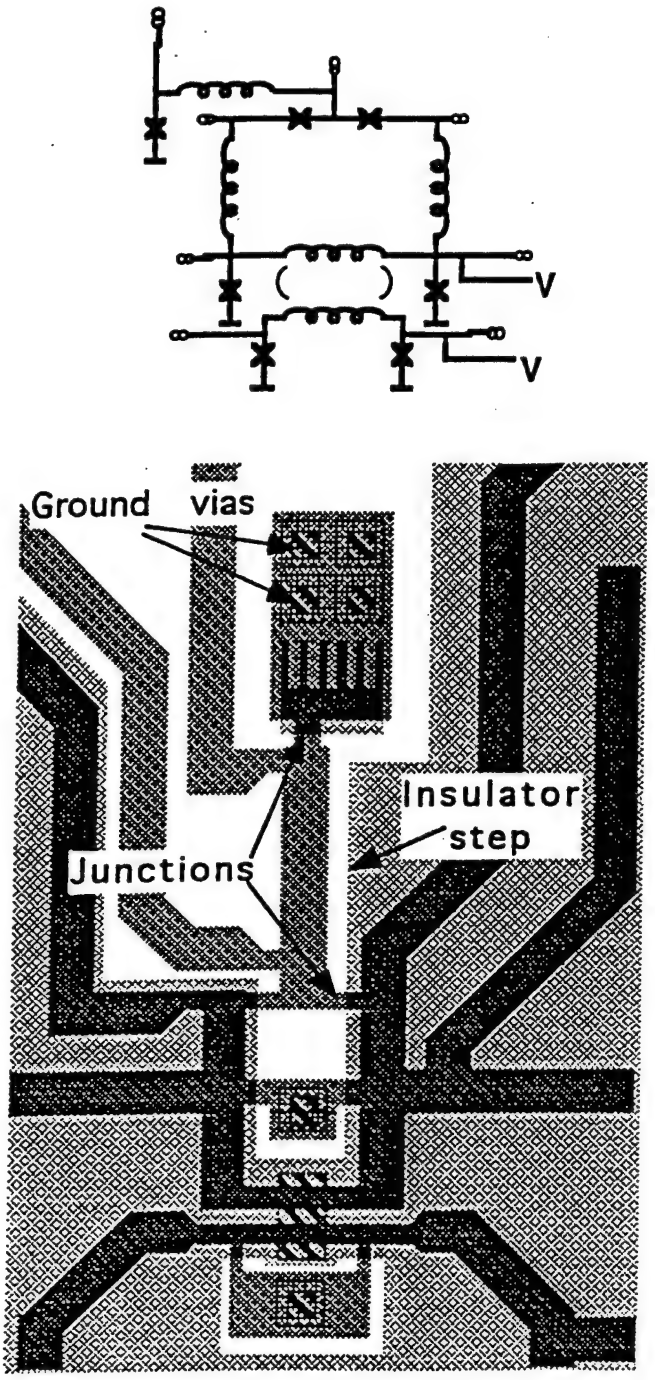

Fig. 2 Circuit diagram and mask layout of a T-flip-flop.

The use of SEGB junctions in our process requires an even number of junctions between each pair of ground contacts. Where circuit designs differed from this process requirement, an additional, interdigitated, junction was introduced as shown at the top of Fig. 2.

Circuit inductances were scaled from the SQUID measurements of Forrester et al [3], taking into account differences in the dielectric layer thickness.

Included in the circuit of Fig. 2 is a readout SQUID magnetically coupled to the storage inductor of the TFF. Coupling is achieved through a common ground plane hole following Chang [6].

IV. Conclusions

We have identified a process for the fabrication of HTS digital circuits using step-edge-grain-boundary junctions. The process incorporates multilayer YBCO films for inductance control, arbitrary location of Josephson junctions, and resistors. With the addition of an additional superconducting wiring level, the process is extendible to complex circuits, limited only by process yields. Simple SFQ circuits using this process have been designed and fabricated. Measurements of these circuits are in progress.

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HIGH-T_c SNS EDGE JUNCTIONS FOR DIGITAL CIRCUIT APPLICATIONS

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ABSTRACT

We have fabricated high-T_c superconductor/normal-metal/superconductor (SNS) weak links in an edge geometry with integrated $YBa_2Cu_3O_x$ (YBCO) groundplanes using a process which incorporates six epitaxial layers, including a Co-doped-YBCO normal-metal interlayer. The SNS edge junctions were produced using films deposited by both off-axis sputtering and pulsed laser deposition. These devices exhibit narrow J_c spreads and high I_cR_n products in a current density regime suitable for Single-Flux-Quantum (SFQ) circuits. This device technology has been used to fabricate high performance SQUIDs and small-scale SFQ digital circuits.

KEY WORDS: SNS, Josephson junction, edge junction, groundplane, $YBa_2Cu_3O_x$

INTRODUCTION

SFQ logic offers the potential of 10 Ghz operation combined with very low power dissipation. Demonstration of SFQ circuits requires the fabrication of high quality Josephson junctions in a multilevel epitaxial process. In particular, junctions with high critical-current - normal-state-resistance (I_cR_n) products (>200 μV), narrow critical current spreads (<15%), and low junction and interconnect inductances are needed. The inductance constraints are most readily satisfied by incorporation of a superconducting groundplane. We have recently reported on the fabrication of high performance SNS edge junctions and SQUIDs integrated with YBCO groundplanes [1,2] and good progress in this area has also been made by other groups [3,4]. In this paper we present an overview of our work with new details on processing, as well as recent junction, SQUID, and circuit results.

PROCESS DETAILS

The YBCO, $SrTiO_3$ (STO), and Co-doped YBCO (usually $YBa_2Cu_{2.79}Co_{0.21}O_x$ - 7% Co), films used in this work were deposited by off-axis rf-magnetron sputtering or by pulsed laser deposition (PLD). To date, sputtering has been used for deposition of every layer for some chips, and is usually utilized for growth of the groundplane and groundplane-insulator. Details of the sputter deposition were given in an earlier paper [1]. Our PLD film process is less mature than our sputtering process, and has primarily been used for YBCO base electrode deposition and for growth of the normal metal and counterelectrode layers. A description of the PLD film process is given in Ref. [2]. The RMS roughnesses of PLD YBCO films in 10x10 μm AFM scans were ≈ 30 - 50 Å compared to ≈ 10 - 30 Å for the best sputtered films. While the PLD YBCO films were not as smooth as the best off-axis-sputtered films, we have found that our PLD film process appears to be more stable overall, and further optimization of the PLD process is expected to lead to smoother films.

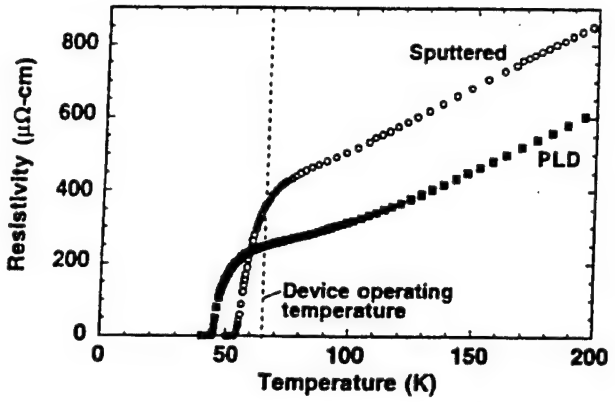

Fig. 1. Resistivity versus temperature for typical 7% Co-doped YBCO thin films produced by off-axis sputtering and laser ablation.

The Co-doped YBCO normal-metal films were grown by both sputtering and PLD under slightly different conditions from YBCO [1, 2]. These deposition parameters produced films with the best electrical properties, although the Co-YBCO films generally contained more outgrowths than optimized YBCO films. We found that the PLD-optimized $YBa_2Cu_{2.8}Co_{0.2}O_x$ thin films usually had electrical properties closer to bulk values than the sputtered films as shown in Fig. 1, with transition temperatures more suitable for the desired circuit operating temperature of 65 K. The broader, higher-temperature transition seen with the sputtered Co-YBCO films is believed to be due to inhomongeneous Co incorporation. Nonetheless, both the sputtered and PLD grown Co-YBCO films have been used for fabrication of high quality SNS junctions. We have also fabricated SNS edge junctions using $Y_{0.7}Ca_{0.3}Ba_2Cu_3O_x$ or $Y_{0.75}Pr_{0.25}Ba_2Cu_3O_x$ as normal metals [5], but the Co-doped YBCO devices had I_cR_n products slightly larger than the Pr-YBCO junctions and about four times higher than the Ca-YBCO devices, so most of our efforts have concentrated on Co-doped-YBCO SNS junctions.

The majority of our work to date has focused on fabricating SNS edge junctions above buried groundplanes using the two configurations shown in Fig. 2. The "double-via" approach shown in Fig. 2a) uses two separate via patterning steps to make contact to the groundplane and base electrode resulting in separate patterning and epitaxial growth of the groundplane, the groundplane insulator, and the base electrode bilayer. Because epitaxial growth over a patterned film is quite sensitive to surface cleanliness of the underlayer, the yield of such a sequence of patterning and growth steps can be reduced, even with the cleaning procedure described in [1]. Fig. 2b) illustrates an alternate "single-via" approach in which an *in-situ*

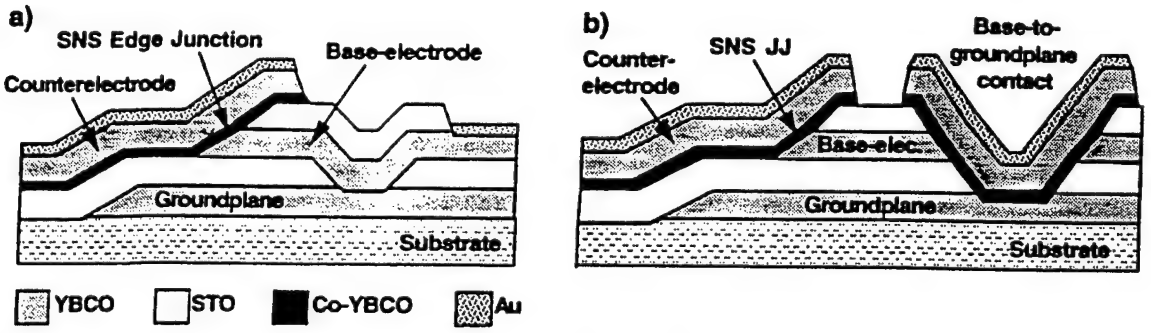

Fig. 2. Schematic cross sections of YBCO/Co-YBCO/YBCO SNS edge junctions integrated with buried YBCO groundplanes a) "Double-via" process, b) "Single-via" process.

STO/YBCO-base-electrode/STO trilayer is grown over the patterned groundplane. In this case contact between the base electrode and groundplane is made through large-area SNS junctions defined by a single via through the trilayer combined with counterelectrode "plugs" patterned at the same time as the junctions. The advantages of this process are a reduced number of mask layers and *in-situ* growth of the base electrode trilayer, an inherently higher yield approach than the double-via process. Potential disadvantages are reduced circuit layout flexibility and lower-J_c via contacts. At the present we are using both processes to produce high quality junctions with groundplanes.

Both the single and double-via processes are based on a buried groundplane configuration to minimize process exposure of completed SNS devices. However, it should be noted that there is no inherent reason to prohibit the use of groundplanes on top. Putting the groundplane above the junctions simplifies the processing, because groundplane morphology is no longer critical. In addition, fabricating the junctions directly on the substrate may ultimately lead to tighter device parameter spreads, and the groundplane and groundplane insulator serve as passivation layers for the buried junctions. We have begun experiments with groundplanes over SNS devices, with promising initial results. In this case we continued processing SNS junctions patterned without Au contacts or buried groundplanes by growing an STO layer and patterning via contacts to the buried electrodes. Finally the YBCO groundplane was deposited and patterned, and Au contacts were defined. Results are discussed in the next section.

ELECTRICAL RESULTS AND DISCUSSION

SFQ circuits require inductance (L) - I_c products on the order of a single flux quantum, $\phi_o \approx$ 2000 pH-μA. Because typical microstrip inductances are about 1 pH/□ [1,2], conventional SQUID layouts point to critical currents of a few hundred μA, with the lower limit set by thermal noise considerations. Fabricating devices with lower I_c values is accomplished by using thicker N-layers, which leads to an associated reduction in the I_cR_n products.

Fig. 3 shows data for all eight 4-μm-wide SNS edge junctions on a standard test chip. These devices have no groundplanes and all layers were deposited by off-axis sputtering including the 100 Å Co-doped-YBCO normal metal layers. At 65 K the devices exhibit high quality I-V

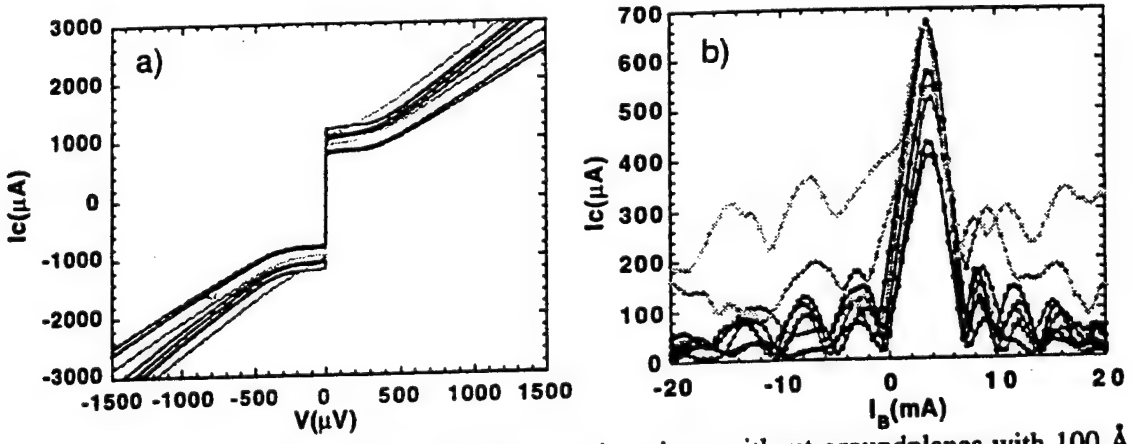

Fig. 3. Data for the eight 4-μm-wide SNS edge junctions without groundplanes with 100 Å Co-doped-YBCO normal metal layers on a standard test chip. a) I-V characteristics at 65 K. On average $J_c = 2.4 \times 10^3$ A/cm^2 with a 1-σ spread of 15% and $I_cR_n = 570\mu V$. b) I_c vs. magnet current at 70 K for a field applied normal to the substrate.

characteristics qualitatively consistent with the resistively-shunted junction (RSJ) model as shown in Fig. 3a). At this temperature the average device parameters and spreads for these junctions were: $J_c = 2.4 \times 10^5$ A/cm^2, 1-σ = 15%; I_cR_n = 570 μV, 1-σ = 7%; and $R_nA = 2.4 \times 10^{-9}$ Ω-cm^2, 1-σ = 11%. The critical-current magnet field modulation data for these devices at 70 K are presented in Fig. 3b). Six out the eight devices show close-to-ideal Fraunhofer patterns, and even the other two devices have clean central peaks, which indicates conduction through the normal metals layers is fairly uniform. For this particular chip, the average current density and critical currents are larger than required for SFQ circuit applications. We have also demonstrated tight critical current spreads in devices with SFQ-compatible critical currents. Data from one such chip was presented in [2]. In that case the average I_c was approximately 210 μA with a 1-σ spread of 16% and an average I_cR_n product of 181 μV. This combination of narrow I_c spreads with device parameters suitable for small-scale SFQ circuits is an important demonstration for the feasibility of SFQ digital applications.

As discussed earlier, another key requirement for SFQ circuits is the incorporation of superconducting groundplanes. We have fabricated high quality Josephson junctions integrated with groundplanes in several configurations. Fig. 4.a) shows I-V data at 65 K for the four 4-μm-wide SNS edge junctions fabricated over YBCO groundplanes on a standard test chip using the "double via" process (Fig. 2.a)). The 150 Å Co-doped-YBCO normal metal layers were deposited by off-axis sputtering. The average device parameters for these junctions are: $J_c = 1.27 \times 10^5$ A/cm^2 with a 1-σ spread of 20%; I_cR_n = 587 μV with a 1-σ spread of 15%; and $R_nA = 4.8 \times 10^{-9}$ Ω-cm^2 with a 1-σ spread of 24%. The effectiveness of the groundplanes was qualitatively verified by magnetic-field I_c modulation studies. Fig. 4b) is a plot of I_c vs magnet current for a field perpendicular to the substrate at 77 K for junctions with and without a groundplane patch. Both curves approximate the expected sin(x)/x I_c modulation, but the junction over the groundplane exhibits a modulation period about four times that of the other junction, demonstrating the magnetic shielding effect of the superconducting film.

The junction parameters of the devices shown in Fig. 4a) are essentially identical to those for junctions without groundplanes: fabricating the edge junctions above the patterned groundplane and groundplane insulator did not degrade the device quality. However, it should also be noted that for some device chips fabricated over rougher YBCO groundplane films (RMS roughness ≈ 30-50Å) the average J_c has been higher and the average R_nA product lower

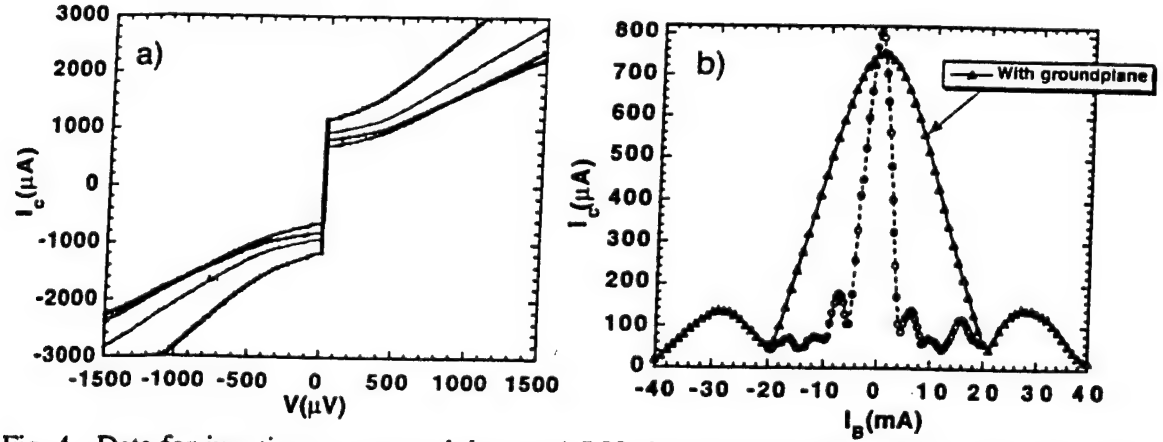

Fig. 4. Data for junctions on groundplanes. a) I-V characteristics at 65 K for the four 4-μm-wide SNS edge junctions with groundplanes with 150 Å Co-doped-YBCO normal metal layers on a standard test chip. b) I_c vs magnet current at 77 K for two devices with 100Å Co-YBCO layers, with and without groundplane patches.

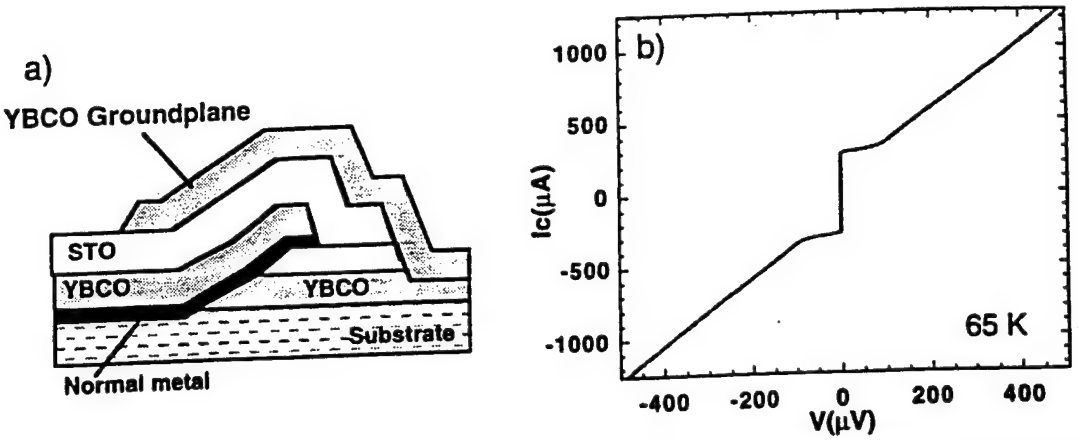

Fig. 5. a) Schematic cross-section of SNS edge junction with an epitaxial insulator and YBCO groundplane added above the device. b) I-V characteristics at 65 K for an SNS edge junction with a 50 Å PLD Co-YBCO N-layer integrated with a groundplane over the junction.

relative to junctions without groundplanes [2]. This may indicate that rougher growth in the upper layers of our multilevel structures is leading to normal metal edge coverage problems. These results emphasize the importance of using the smoothest possible groundplane and insulator films in multilayer structures with buried groundplanes.

We have also fabricated SNS edge junctions in a buried *junction* geometry as sketched in Fig. 5a). While some chips processed with this approach have shown depressed operating temperatures [2], recent devices fabricated with groundplanes above the junctions exhibit RSJ I-V characteristics at 65 K, as shown in Fig. 5b). In this case chips processed with groundplanes on top had I-Vs equivalent to companion chips which had no groundplane added, demonstrating that the junctions can survive high temperature processing. We are in the process of studying groundplane effectiveness in this configuration.

The double-via buried groundplane approach has been used to fabricate direct-injection SQUIDs [1,6]. The voltage modulation at 65 K of one such device is shown in Fig. 6a) as a function of the control current flowing through a microstrip inductor forming part of the SQUID loop. The maximum voltage modulation at this temperature is ≈ 135 μV. The microstrip inductance can be determined from the period of the voltage modulation curves, and Fig. 6b) is a plot of the microstrip inductance per square as a function of temperature for a set

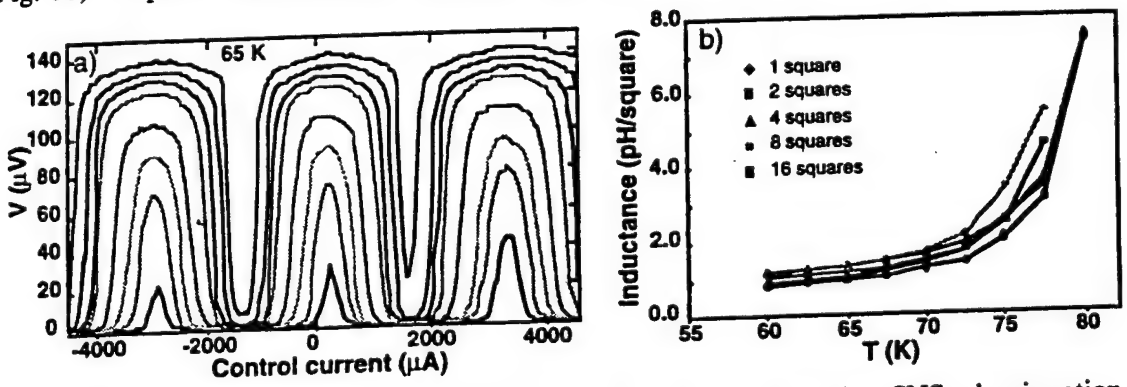

Fig. 6. a) Voltage modulation vs. control current for a direct injection SNS edge junction SQUID with integrated groundplane at 65 K at various bias levels. b) Temperature dependence of the microstrip inductance per square extracted from the V-ϕ curves for five SQUIDs.

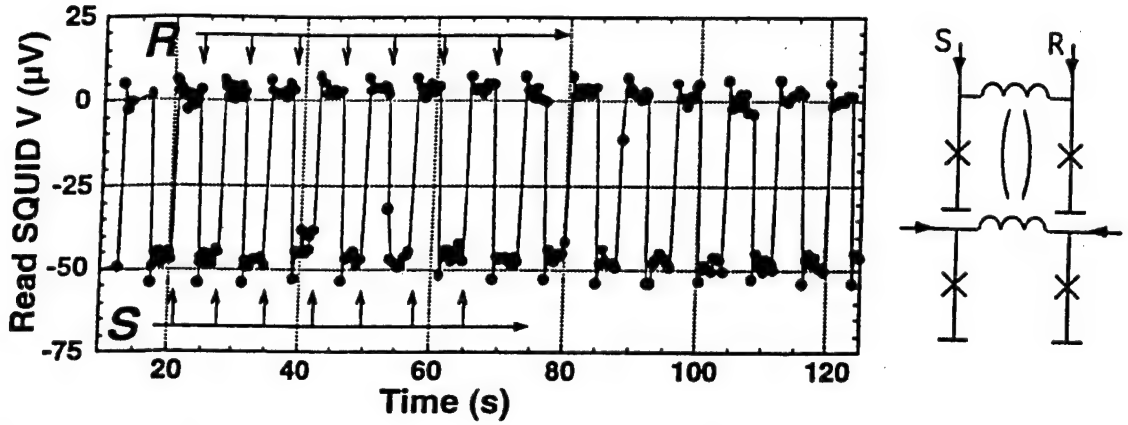

Fig. 7. Low speed test data and schematic diagram for an SNS edge junction R/S flip-flop at 65 K. The Read SQUID modulates by approximately 50 μV in response to flux quanta stored in the Data SQUID by set and reset pulses.

of SQUIDs with different microstrip lengths. The inductance is about 1 pH per square at 65 K, which is suitable for fabrication of SFQ circuits.

We have begun using this multilayer device technology to produce small-scale SFQ circuits, including R/S flip-flops with 4 junctions and a 1-bit A/D converter with 10 junctions [7]. Low speed test data for an SNS R/S flip-flop are shown in Fig. 7. The data show Read SQUID voltage modulation of ≈ 50 μV in response to flux quanta stored in the Data SQUID by set and reset pulses. This voltage level is about a factor of ten larger than previous test results with Step-Edge Grain Boundary (SEGB) circuits due to the larger I_cR_n products of the SNS devices [8]. Mask and test setup modifications are being made to allow GHz testing of the flip-flops.

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Long Term Stability of YBCO-Based Josephson Junctions*

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Abstract—We report on a study of long term aging in three different types of $YBa_2Cu_3O_{7-x}$ Josephson junctions. Junction aging will affect the choices made in integrating this technology with actual applications. The junction types used in this study are (a) Co-doped barrier edge SNS junctions, (b) noble-metal SNS step-edge junctions, and (c) bicrystal junctions which are either unpassivated or passivated *in situ* with a normal metal shunt or an epitaxial insulator. While all the junctions show degradation, for some the long term survival rate is encouraging.

I. Introduction

High T_C Josephson junctions are the critical components of many superconductive circuits. Technological applications demand junctions that can be reproducibly fabricated and can withstand the rigors of thermal cycling and long term storage. To date, various research groups have developed reliable processing methods for producing high-T_C thin film electronic devices utilizing Josephson junctions based on $YBa_2Cu_3O_{7-x}$ (YBCO) [1]. However, YBCO thin films degrade with exposure to atmospheric water vapor [2,3] and are also susceptible to surface deoxygenation. These critical issues must be addressed in order to produce junctions that are degradation-resistant and oxygen-stable. There are many examples of protective layers applied to YBCO films that improve the films' long term stability. Depending on the application these layers can be metallic or insulating [3,4], and their effect on the YBCO films vary. In contrast, there is little information regarding the use of protective layers on junctions. We have reported on the protective qualities demonstrated by *in situ* metal shunt layers on bicrystal junctions [5] and the use of STO insulating layers to provide similar protection [5,6]. In this study we report on the aging of three different junction types for which we recorded changes in junction critical current (I_C) and in normal resistance (R_N) over several years. The junction types used in this study are: (a) Co-doped barrier edge SNS junctions ("ramp edge"), (b) noble-metal "step-edge SNS" junctions, and (c) bicrystal grain boundary junctions ("BiGBJs"). This study attempts to establish broad trends indicative of junction aging leading to failure or variation of junction parameters beyond those necessary for the desired applications. While we observed changes in junction characteristics with time, in general, these changes were typically much less than 30%.

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II. Experimental

A. Fabrication Overview

The junction fabrication techniques are described below. A cross-sectional view of each junction is shown in Fig. 1.

(a) *Ramp Edge:* Co-doped barrier edge SNS junctions [Fig. 1a].
We present the results of a single chip with 18 junctions of nominal 3 μm width. The SNS edge junctions [7] were grown with off-axis rf magnetron sputtering of the YBCO base electrode and $SrTiO_3$ (STO) base-electrode-insulator bilayer. The ramp edge was patterned by Ar ion milling and cleaned with 100-eV *in situ* Ar ion milling just prior to N-layer deposition. A 10 nm thick $YBa_2Co_{0.2}Cu_2O_x$ N-layer and YBCO counter electrode were also deposited as a bilayer by rf magnetron sputtering. A Au contact layer was deposited *in situ* after counter electrode growth.

b) *step-edge SNS:* Noble-metal SNS step-edge junctions [Fig. 1b].
The step-edge SNS junctions were fabricated by depositing a thin film of YBCO across a step that had been etched into a substrate. Off-axis sputter-deposition was used to produce a film with the c-axis oriented normal to the plane of the substrate. The sharp step-edge produces a break in the superconducting film, exposing a-axis oriented superconductor. The normal metal, either Ag or a Ag-Au alloy, is then *in situ* sputter-deposited such that it covers the step and joins the two superconducting banks. The proximity effect coupling between superconductor and normal metal thus takes advantage of the longer superconducting coherence length afforded by the exposed a-axis oriented material [8,9]. We present the results of five individual chips with seven junctions each of 3, 6, 9 μm width.

(c) *BiGBJs:* Bicrystal grain boundary junctions [Fig. 1c].
The bicrystal junctions were fabricated on commercially purchased [001] oriented STO and sapphire bicrystals with misorientation angles of 24°. A c-axis oriented YBCO film 100 nm thick was deposited with KrF pulsed laser

deposition (PLD). Where an insulating passivation layer was used over the YBCO, it consisted of a 100 nm thick STO layer that was laser ablated *in situ* . Where a normal metal shunt layer was used, it consisted of a dc sputtered Au film of 35 nm thickness deposited *in situ* at 100 °C. The sapphire bicrystal substrate had an initial 20 nm thick CeO_2 buffer layer. Epitaxial, single-orientation growth of all CeO_2 and YBCO layers was confirmed with x-ray diffraction (XRD) analysis. All GBJs were fabricated by patterning microbridges into the YBCO layer using standard photolithography and Ar^+ ion beam etching. The specifics of the fabrication process are described elsewhere [5]. We present the results from one STO-protected bicrystal, and one Au-protected bicrystal. Each sample consists of 14 junctions total, with 7 junctions each of nominal 4 μm and 8 μm widths.

B. *Measurement Issues*

In a study of this nature, involving samples from three separate laboratories, it is necessary to carefully document the conditions underwhich the samples were (i) stored, (ii) thermally cycled, and (iii) electrically measured, so as to provide a meaningful comparison.

(i) In all cases the chips were stored in dessicators that were regularly exposed to atmosphere when opened. The dessicator environment for the step-edge SNS junctions included an Ar-pressurized atmosphere and for the ramp edge junctions the dessicator was over-pressurized with N_2. All samples were fabricated as described and tested, stored and retested periodically. Sample S92-66 had a photoresist layer applied to it after the first recorded test.

(ii) All measurements were carried out in magnetically shielded liquid He or liquid N_2 Dewars. The sample under test was mechanically clamped to the coldstage of the probe and magnetically shielded before being submerged into the dewar. In the case of the ramp edge junction chip, the sample itself was heat-sunk to the probe coldstage using thermal grease. The temperature difference between sample and thermometer was less than 0.5 K. Where applicable, the temperature was monitored and controlled by a thermometer attached to the coldstage near the sample mount location. The thermometer was periodically calibrated against liquid N_2 and liquid He over the several year time span. The thermometer accuracy was known within 0.1 K. Temperature stability and reproducibility are very important: for example, a difference of 1% in temperature between sample and thermometer could result in a critical current change of 6% for the ramp edge junctions. To prevent water vapor damage, during the warming cycle the probe remained in a positive pressure of He or N_2 gas.

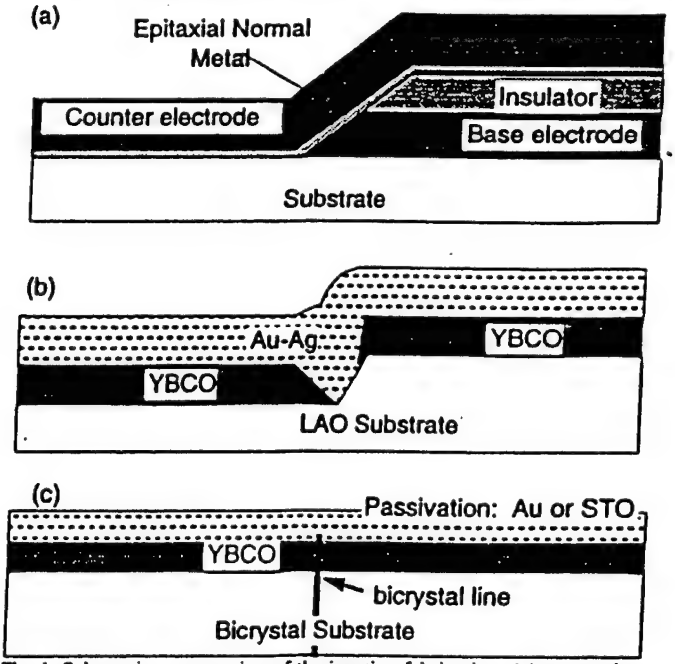

Fig. 1. Schematic cross section of the junction fabrication. (a) ramp edge junction, (b) step-edge SNS junction, and (c) bicrystal grain boundary junction.

(iii) Care must be taken to prevent the trapping of magnetic flux in the junctions and in the superconducting leads. The presence of trapped flux during measurements affects the junction critical currents by applying a magnetic field bias to the Josephson device, leading potentially to as much as a 100% reduction in I_C. To prevent this, the junctions must be cooled in the absence of any magnetic fields. Additionally, it is possible to drive the junction leads into a normal state with too large a bias current, again trapping magnetic flux in the junction. When this occurs the affected junction must be taken above its critical transition temperature and recooled.

III. Results

We reported elsewhere the observation of numerous failures in bicrystal junction samples without any protective layers [5]. On several bicrystal junctions chips, individual junctions with exposed YBCO failed perhaps due to electrostatic sensitivity, environmental exposure, or thermal cycling. These junctions have greater sensitivity to electrostatic discharge, rendering them permanently damaged with regions of high resistivity. Additionally, these unprotected junctions have greater susceptibility to water vapor damage through their exposed surfaces and the exposed grain boundary. In contrast, for the samples presented here from all three sources, no total failures were observed and changes of much less than 25% in junction parameters were typically seen.

In all three laboratories critical currents and normal resistances were measured and archived. The same samples were subsequently remeasured after varying periods of time. Figure 2 is a summary of the on-chip data from (a,b) the ramp edge junctions, (c,d) the step-edge SNS junctions, and (e,f) the BiGBJs. The data shown are for the initial measurement and any subsequent remeasurements of the particular junction set. The I_C and R_N values are normalized to junction width for the step-edge junctions. For the ramp junctions and the BiGBJs they are represented by the critical current density (J_C), and the resistance-area product (R_NA). The I_C and R_N distributions change very little over time; junctions with larger I_C and R_N tend to remain larger at each remeasurement.

Figure 3 is a summary of the data from the samples used in this study. Representative samples were selected for each type of junction, and from two different substrates in the case of the bicrystals. The change in averaged I_C and R_N for all junctions on a given chip is shown relative to its

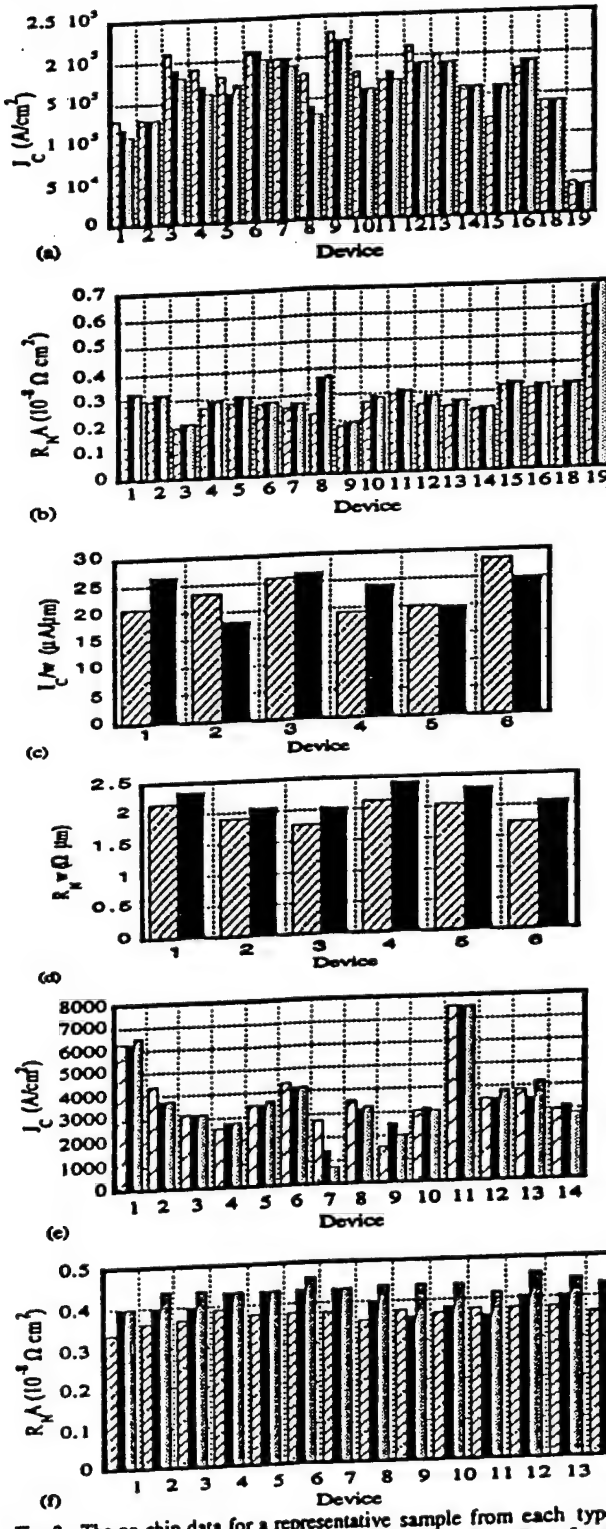

Fig. 2. The on-chip data for a representative sample from each type of junction: (a,b) J_C, R_NA for ramp edge junctions; (c,d) I_C/w, R_Nw for step-edge SNS; and (e,f) J_C, R_NA for BiGBJs. The shaded bar is the original data measurement and the gray bar is the most recent measurement. For 2a,b and 2e,f: the black bar represents an intermediate measurement.

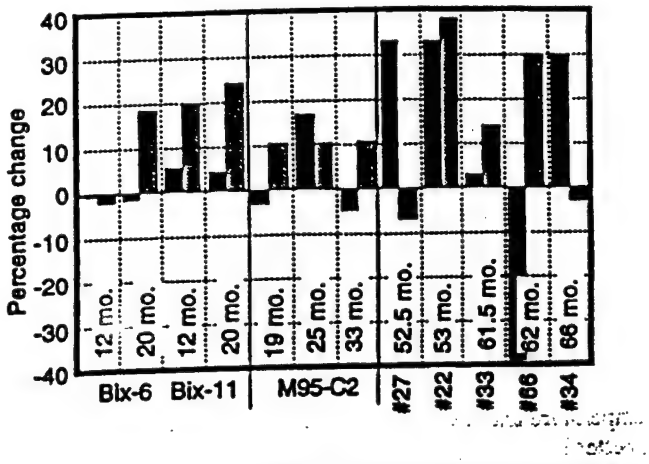

Fig. 3. Percentage change (relative to the initial measurement) in the averaged I_C (black bar) and R_N (gray bar) of all the junctions on a given chip.

initial measurement. In this manner, a change over time is presented with each subsequent measurement. The junction measurements spanned as much as 5 years.

Changes in laboratory measurement technique over the time span can cause data measurement variations that introduce systematic errors which make it difficult to put statistically significant error bars on the average measurements at a level better than approximately 5%. Although this is a small sample group, we can use it to identify trends in the data and expose any large deviations from average behavior. In samples from all three groups, the trend in R_N change is positive.

The average changes in I_C are more complex and vary with junction type, measurement reliability, and extrinsic effects such as storage conditions. The ramp edge junctions show a small decrease in I_C as do the BiGBJs on sapphire. The 25 month ramp edge junction measurement (sample C2) shows a large increase in I_C, whereas the 33 month remeasurement shows a small decrease relative to the first measurement. Re-examination of the measurement conditions has revealed that there was poor thermal contact between the sample and the temperature control block, resulting in a temperature difference of 1.8 K. This temperature change caused the shift in I_C shown in Fig. 3, an example of one of the experimental issues discussed earlier. Thus, the ramp edge junction data demonstrate only a small average decrease in I_C. The STO-protected BiGBJs and the step-edge SNS junctions both have an increase of I_C over time. In the case of the step-edge SNS junctions the I_C increase was about 30%, for the STO bicrystal the I_C increase was about 10%.

IV. Discussion

The ramp edge and step-edge SNS junctions in this study had barrier and/or counter-electrode layers deposited *in situ* as part of their junction geometry. In the case of the BiGBJs, additional *in situ* layers of STO or Au were deposited. The vertical structure of the junctions seen in Fig. 1 demonstrate the "self-passivated" nature of these junctions; in all cases the lack of junction surface exposure

protects them from more severe degradation. The regions that remain vulnerable to attack are the edges that expose the ab-planes of the YBCO. Decreases in I_C and corresponding increases in R_N can result if the overall junction cross-sectional areas are decreasing as damage to the YBCO encroaches inward from the edges. Degradation from the edges could be minimized by covering the affected areas with a passivating layer. Care must be taken in choosing the passivation material, since most chemical and thin film processes are also potentially damaging to the YBCO. It is possible that the very large change in sample S92-66 is due to the use of a spun-on photoresist layer left on the chip during its long period of storage.

The junction resistance is independent of sample temperature and insensitive to trapped flux and is therefore a better indicator of changes in the junction over time than is I_C. Increasing R_N trends were observed for all three types of junctions. For the step-edge SNS junctions, the measurement time scale is at least twice as great as that of the other two types represented here. The greater increase observed in R_N for step-edge SNS junctions may be due to their age or to the use of Ag or Ag-Au alloy as the shunting layer. With its greater reactivity, Ag can corrode over time increasing the resistance of the shunting path parallel to the junction interfaces. The ramp edge junctions with an epitaxial oxide normal layer at the interface will not react in this fashion. Similarly, the passivated BiGBJ samples do not incorporate other layers that are sensitive to oxidation or corrosion.

The I_c increases observed in the BiGBJs and step-edge SNS junctions cannot be explained by a simple area loss mechanism and require further investigation. One plausible model for this behavior is the reoxygenation of an oxygen deficient or disordered layer of YBCO at the junction interface. Studying these junctions over very long periods of time would be valuable in estimating such reoxygenation. For the step-edge SNS junctions, the junction interface region is imperfect, resulting in a high interface resistance. We conjecture that, with more initial disorder, these junctions will be more prone to self-annealing, resulting in a larger observed increase in I_c. The ramp edge junction with its epitaxially clean interface exhibits only a small decrease in I_c.

Other experiments that might be explored are junction oxygen anneals. Oxygen plasma anneals performed on ramp edge junctions result in an increase in junction I_c with a small decrease in R_N [10] possibly due to a reversal of junction degradation damage or by encouraging oxygen diffusion to the deficient junction interfaces. Additionally, oxygen electromigration studies [11] may help clarify the significance of oxygen mobility to the long term stability of junction characteristics.

V. Conclusions

This study of the junction aging effects and stability, demonstrates that these junctions have survived over many years and that they show sufficiently small changes in their characteristics that they can be considered adequate for many applications. Based on an average increase in R_N, these junctions show some degradation in junction characteristics which might be reduced by use of an appropriate passivation layer. Other work has shown that oxygen diffusion contributes to changes in junction critical currents, leading us to speculate that such diffusion could be the factor responsible for the observation of occasional increases in average I_c.

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Multilayer Edge SNS SQUIDs for Digital Circuits

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Abstract — **We have fabricated and characterized direct-injection High Temperature Superconducting (HTS) SQUIDs using a six-epitaxial-layer process which integrates edge geometry superconductor-normal-superconductor (SNS) junctions with an HTS ground plane. The period of the SQUID threshold curves was used to infer microstrip inductances of approximately 1 pH/□ at 65 K. Total SQUID inductances as low as ≈ 5 pH were inferred from the measured critical current modulation depth. A novel junction geometry was used in some devices to reduce the parasitic inductances of the junction leads by approximately 1 pH. Maintaining such low inductances is particularly important for Single Flux Quantum digital circuits.**

I. Introduction

Digital circuits based on HTS Josephson junctions have the potential for GHz operation with power dissipation of microwatts per gate, operating at temperatures attainable with compact cryocoolers (e.g. 65 K). To realize this potential it is necessary to develop a fabrication process based on reproducible, manufacturable, high I_cR_n junctions. In addition, for maximum circuit layout flexibility, it is desirable to use an integrated groundplane to minimize inductance, L, in order that the product LI_c be approximately equal to the flux quantum, Φ_0. For SFQ circuits in particular, thermal noise constraints dictate that I_c should be as large as possible, while meeting the constraint that $LI_c = \Phi_0$.

For certain applications, such as A/D converters, we believe that a reasonable compromise is to have $I_c \approx 0.5$ mA, so that a typical inductance would be 4 pH. Such low inductances can be achieved in a single HTS layer by using narrow slit inductors, patterned with, for example, e-beam lithography [1]. However this approach suffers from parasitic mutual inductance between slits, and does not allow superconducting crossover interconnections, which are required for circuits of even modest levels of integration. The use of the base electrode of an edge (or "ramp") junction as a local ground to produce low inductances has also been demonstrated [2], but this also is not sufficiently flexible for more complex circuits.

We have recently reported on the fabrication of SNS edge junctions and SQUIDs with an integrated YBCO ground plane, using a flexible process with six epitaxial layers[3]. We have found the critical current uniformity of such edge junctions to be superior to other approaches such as grain boundary junctions.

Here we present more detail on SQUID inductance measurements, and in particular the inference of total SQUID inductance from the depth of critical current modulation. In addition we present results for a modified process which reduces parasitic inductances associated with the narrow junction leads.

II. Device Fabrication

The two baseline fabrication processes used are illustrated in Fig. 1, and are described in detail elsewhere [3],[4]. Epitaxial YBCO, Co-doped YBCO, and $SrTiO_3$ (STO) films were deposited by off-axis rf magnetron sputtering from stoichiometric targets onto $NdGaO_3$ substrates. Patterning was performed by ion milling, with the substrates mounted on a tilted, rotating, water cooled sample stage, using a reflowed photoresist mask to obtain edge tapers of ≈ 25–30°.

For the "double via" process of Fig. 1(a) there are four separate high-temperature growth steps, each followed by an ion mill patterning step and an ion cleaning. A YBCO ground plane (typically ≈ 200 nm thick) is deposited and patterned first, followed by the ≈ 250 nm STO groundplane insulator. The third deposition is of the 100–200 nm base electrode, followed in-situ by a STO cap layer. The tapered edges required for junction formation are then milled in this bilayer. Finally the N-layer, typically 10-30 nm of $YBa_2Cu_{2.79}Co_{0.21}O_x$, and a 200 nm thick YBCO counterelectrode, with an in-situ Au contact layer, are

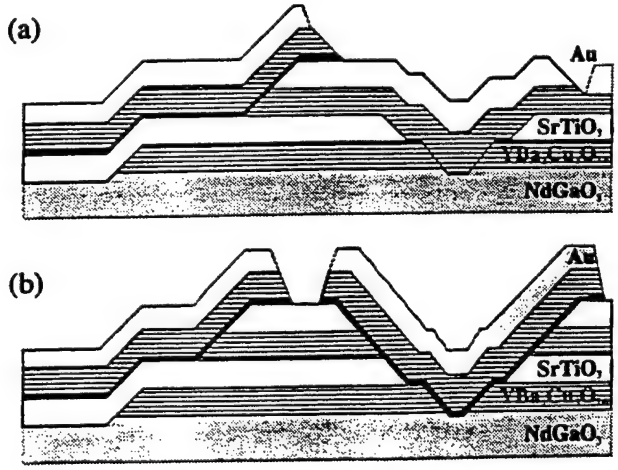

Fig. 1. Schematic cross sections of the two processes used to fabricate edge SNS junctions and SQUIDs over groundplanes. The "double via" process, (a), reduces the number of separate epitaxial growth steps compared to the "single via" process, (b), but necessitates that ground contacts be large area junctions.

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deposited and patterned. In this process contacts to ground are made directly from the base electrode through vias in the STO groundplane insulator. If desired, vias are also milled through the base electrode cap layer, and filled by an ex-situ Au deposition, to provide direct electrical contact to the base electrode.

The "single via" process is similar to one developed at Conductus [5], and involves only three high temperature depositions because the groundplane insulator is deposited at the same time as the base electrode and its insulator. This trilayer is then patterned twice — once to cut a via hole through the entire trilayer, and once to cut the base electrode edge. Contacts to ground are then completed by a plug of counterelectrode and N-layer, with the disadvantage that such contacts are necessarily junctions, albeit of width significantly larger than the "deliberate" junctions. The advantage is that reducing the number of epitaxial growths steps tends to increase the process reliability.

A photograph of a completed direct-injection SQUID, fabricated with the double-via process, is shown in Fig. 2(a).

III. Measurements

The fabricated 1-cm chips were mounted in commercial 44-pin ceramic chip carriers for measurement. The carrier was inserted into a magnetically-shielded, temperature-controlled cryostat with twisted-pair leads filtered with a cutoff frequency of about 10 Hz. Measurements were performed under computer control.

Flux was applied to the SQUIDs by direct current injection into opposite ends of a microstrip inductor formed by the counterelectrode, the groundplane insulator, and the ground plane. With current I_1 injected in one end and I_2 in the other the control current is given by $I_{cont} = (I_1 - I_2)/2$, and the flux applied to the SQUID is given by $L_\mu I_{cont}$, where L_μ is the microstrip inductance. Typically we measured the SQUID voltage, V, versus I_{cont} at various levels of total bias, I_1+I_2, as a function of temperature. We also measured the critical current, using a voltage criterion of 2 μV, as a function of I_{cont} at a few selected temperatures. Since the leads of the ceramic chip carrier were slightly magnetic we usually observed some shifting of the SQUID threshold curves.

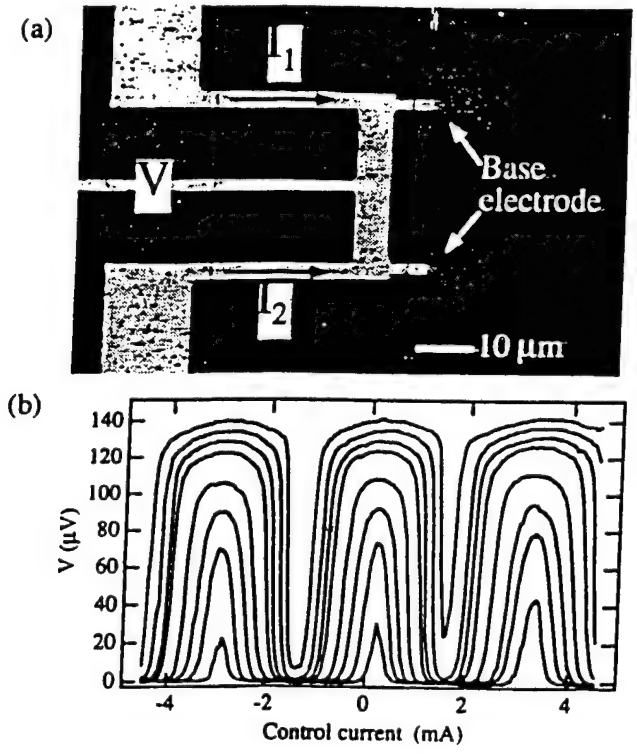

Fig. 2. (a) Photograph of typical direct injection SQUID fabricated with the "double via" process, with definitions of bias currents. Some devices did not have the center tap, in which case the voltage was measured on one of the current leads. (b) Voltage versus control current, at various bias levels, for a typical SQUID at 65 K.

IV. Electrical Results

A. *Voltage modulation and microstrip inductance*

Voltage modulation of a typical SQUID with a short (~1 square) microstrip inductor is shown in Fig. 2(b) at various total bias levels, at 65 K, where this particular device had the following parameters: $I_c \approx 1.75$ mA, $R_n \approx 0.25$ Ω, total inductance $L_{tot} \approx 10$ pH (inferred from I_c modulation depth as discussed in the next section). The maximum voltage modulation is about 135 μV peak-to-peak, with $(dV/d\Phi)_{max} \approx 1.8$ mV/Φ_0. Corresponding values at 77 K were 40 μV and 230 μV/Φ_0, respectively. For the listed SQUID parameters the expected peak-to-peak voltage modulation, using equation 7 of [6], is about 30 μV. The measured value is larger than expected because of strong resonances which we observe in the current voltage characteristics of these SQUIDs (although not in single junctions), which lead to high values of dV/dI in certain bias regions, and thus to higher values of $dV/d\Phi \approx (dV/dI)(dI_c/d\Phi)$.

From the period, ΔI_{cont} of voltage modulation data of the type shown in Fig. 2(b), we calculate the inductance of the microstrip using $L_\mu = \Phi_0/\Delta I_{cont}$. This is shown in Fig. 3 for SQUIDs with various lengths of inductor, normalized to the number of squares between the inside edges of the current leads. Typical values are in the range 1–1.5 pH/□ at 65 K, similar to values we have previously reported for SQUIDs fabricated using a simpler process incorporating step edge grain boundary junctions [7]. As can be seen in Fig. 3 there is an appreciable spread in inductance from one device to another at high temperatures. This is thought to be due to local variations in the T_c of the ground plane and/or base electrode, and thus in the penetration depth, possibly due to incomplete oxidation [8]. The T_c of the these layers was often found to be suppressed to below 85 K, compared to 87 K for the counterelectrode. Diffusion of oxygen through the

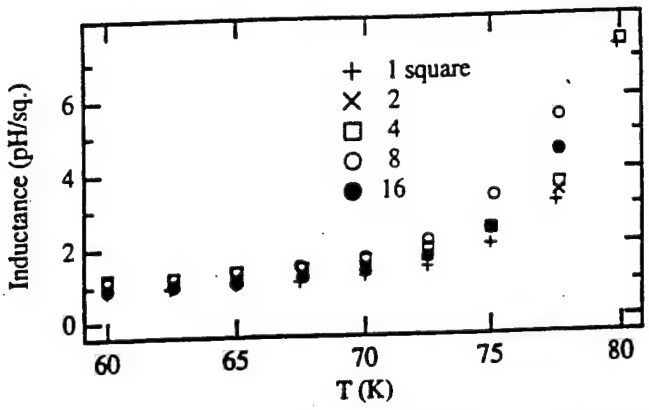

Fig. 3. Microstrip inductance per square inferred from the period of V-I_{cont} curves, for various lengths of microstrip inductor.

insulating layers of such a complex structure is an issue which will require further attention.

B. I_c Modulation and Total Inductance

Although one can in principle infer the total SQUID inductance from the depth of the voltage modulation, the resonances in the I-V characteristics, referred to in the previous section, complicate such an analysis. It is simpler to use instead the depth of critical current modulation.

Typical data are shown in Fig. 4 at three different temperatures. To infer the SQUID inductance from such data we us the following expression [6]:

$$\frac{\Delta I_c}{I_c} \approx \frac{1}{1+\beta_L}\left(1-3.57\frac{\sqrt{k_B T L}}{\Phi_o}\right) , \qquad (1)$$

where, ΔI_c is the measured SQUID critical current modulation depth, and $\beta_L = LI_c/\Phi_o$. The second term in parentheses takes account of the effect of thermal noise currents in the SQUID inductance. Solving (1) for L gives an upper bound on the inductance, since any critical current

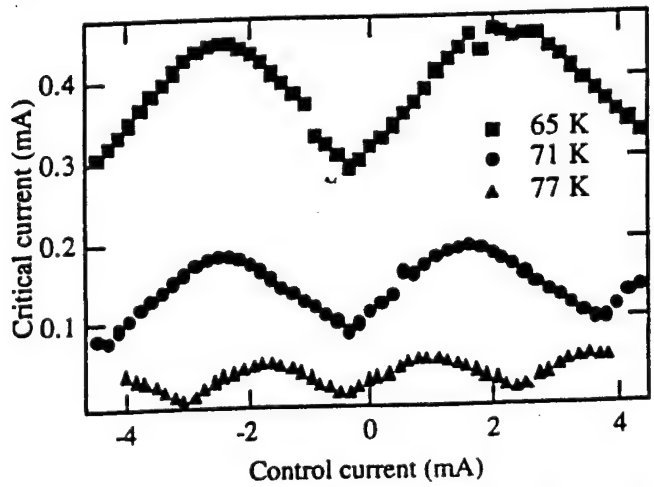

Fig. 4. Critical current versus control current for a typical SQUID. Note that the curves are shifted due to trapped flux.

asymmetry between the two junctions will reduce the modulation depth. The SQUID lobe patterns typically did not show significant skewing so we ignore this correction.

The total inductance inferred from (1) is plotted in Fig. 5(a) for ten different SQUID layouts of the general type shown in Fig. 2(a). They differ in the length of the microstrip inductor, the lengths of the junction leads, and details of the ground contact arrangement. The lowest inductance device is about 5 pH, at 65 K – quite close to the nominal 4 pH goal.

In what follows it is useful to calculate a normalized measure of SQUID inductance which we call the "effective

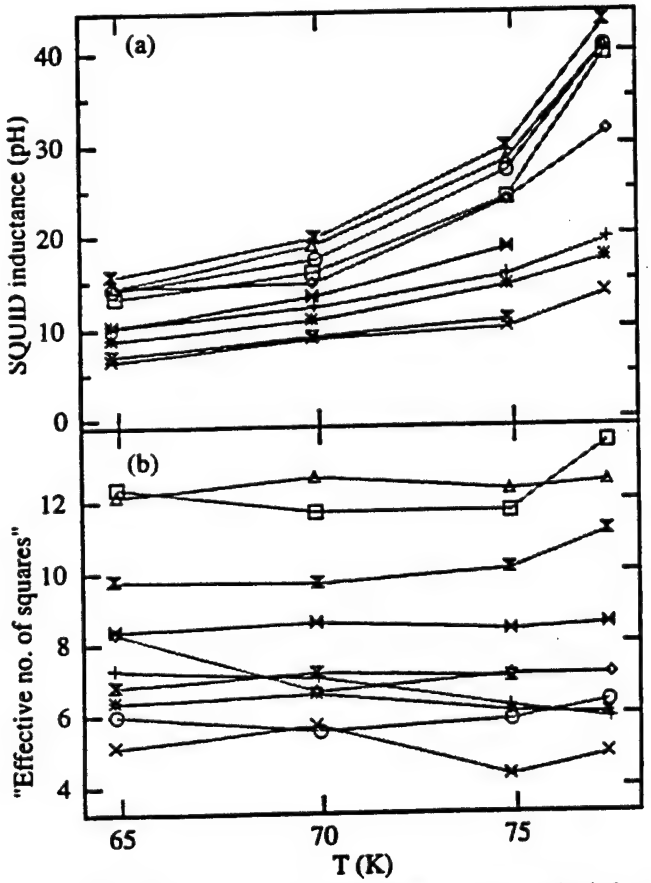

Fig. 5. (a) Total SQUID inductance, inferred from I_c modulation depth, for ten different SQUID layouts. (b) "Effective number of squares", obtained by dividing the total SQUID inductance by the inductance per square. It is essentially independent of temperature, as it should be.

number of squares", $N_{eff} \equiv L_{tot}/L_{\square}$, where $L_{\square}$ is the inductance per square measured from the modulation period. This is useful because it normalizes out variations in the YBCO penetration depth, and therefore allows us to compare inductances of different SQUID layouts from different chips. It is plotted in Fig. 5(b) for the devices of Fig. 5(a), and is found to be roughly independent of temperature, as it should be. In general it agrees well with simple counting of squares in the SQUID layout, although there are some unresolved discrepancies in the smaller SQUIDs which we hope to investigate further.

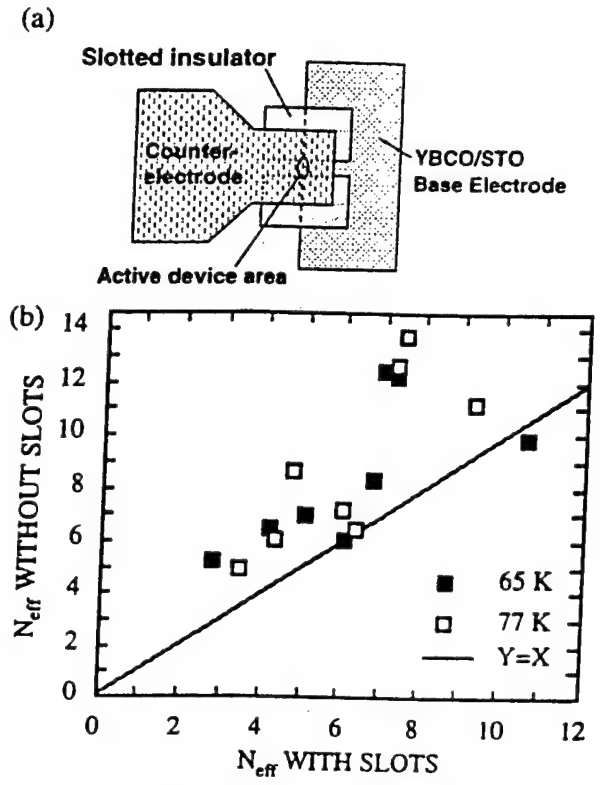

Fig. 6. (a) Schematic diagram of a slot-defined edge junction. (b) Normalized total SQUID inductances, expressed as effective number of squares, for devices fabricated without vs. with slot-defined junctions. The slot junctions reduce the junction lead inductance and thus the SQUID inductance.

V. SQUIDs WITH SLOT-DEFINED JUNCTIONS

A significant fraction of the total SQUID inductance is in the junction leads, which are typically 1.5 – 4 μm wide (in order to obtain critical currents of order 0.5 mA) and 4 – 5 μm long, and therefore contributing ≈ 1 – 3 squares per junction. One approach to reducing this parasitic inductance is to simply make the junction leads shorter by allowing the distance between the base electrode edge and the wide section of the counterelectrode to be reduced. The lower limit on this distance will be set by alignment accuracy and the finite extent of the shallow base electrode edge, and it is probably impractical to reduce it much below 1 – 1.5 μm.

Here we present an alternative or supplementary approach, illustrated in Fig. 6, which we term "slot junctions" [4]. Here the junction width is determined not by the lead width, but by a slot opening in an epitaxial insulator layer deposited and patterned after the base electrode edge is patterned. This allows the junction lead to be much wider than the junction itself, reducing the inductance.

We have tested the concept by fabricating eight different SQUID designs both with and without the use of the slot process. We measured the total inductance and inductance per square for the devices, and calculated N_{eff}. In Fig. 6(b) we plot N_{eff} for the "slotless" devices on the vertical axis, and for the "slotted" devices on the horizontal axis for these eight devices, at 65 and 77 K. Although there is scatter in the data it is clear that overall the slot devices have lower inductance, with an average inductance reduction of approximately two squares, or one square per junction. For example the device which had $N_{eff} \approx 5$ was reduced to ≈ 3 in the slot process. Because these particular devices had a longer penetration depth than usual (about 0.3 μm, compared to the more typical 0.25 μm) the total inductance was still 4.5 pH, but implementation of such a device with higher quality films with 1 pH/□ should result in a 3 pH SQUID.

In addition to reducing the junction parasitic inductance the addition of the slot insulator allows much greater circuit layout flexibility since it allows one to run counterelectrode wiring over the base electrode without forming a junction.

VI. CONCLUSIONS

We have demonstrated that the integration of an HTS ground plane with HTS edge junctions can produce microstrip inductances of 1 pH/□, and SQUIDs with total inductances as low as ~ 5 pH, at 65 K. The demonstrated slot-defined junction process can reduce the latter to about 3 pH for films with 0.25 μm penetration depth. The use of more agressive photolithographic design rules can reduce this further, which will improve the margins of HTS SFQ circuits. The use of the additional slot insulator also makes the process more flexible in that it allows the counterelectrode to be used more fully for wiring over the base electrode.

ACKNOWLEDGMENT

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High-Resistance HTS SNS Edge Junctions

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Abstract—**HTS SFQ digital circuit applications require high resistance HTS Josephson junctions. We have investigated the factors affecting the resistance of SNS edge junctions which use Co-doped Y-Ba-Cu-O as the normal metal layer. Several parameters are found to have a surprisingly large effect on device resistance, including edge angle, base electrode material, and deposition conditions of the normal metal and counterelectrode. Controlling these factors has enabled the fabrication of high-quality, high-resistance (≈1 Ω) SNS edge junctions with 1-σ I_c spreads down to 10% and critical currents and I_cR_n products suitable for SFQ digital applications.**

I. Introduction

High Temperature Superconductor (HTS) digital circuit applications based on Single Flux Quantum (SFQ) logic require the fabrication of high quality Josephson junctions in a multilevel epitaxial process. One HTS junction technology of particular interest has been edge-geometry superconductor/normal-metal/superconductor (SNS) weak links with $YBa_2Cu_{3-x}Co_xO_7$ (Co-doped YBCO) as the normal metal interlayer ("N-layer"). Good progress has been made in integrating edge junctions using Co-YBCO and other normal metal layers with superconducting groundplanes [1-6], but further improvements are needed to build practical digital circuits. In particular, SFQ circuits require junctions with high critical-current - normal-state-resistance (I_cR_n) products (>300 μV), and tight critical current spreads (I_c 1-σ < 10%). SFQ design constraints on LI_c products and thermal noise considerations also point towards SNS critical currents of ≈ 500 μA at 65 K. The bounds on I_cR_n and I_c indicate that device resistances greater than ≈ 0.5 Ω are needed for functional HTS SFQ circuits.

The resistance of an SNS junction is determined by the sum of the resistance of the normal metal layer and the interface resistances. In the "ideal" case of zero interface resistances we can estimate the device resistance for typical device cross-sectional areas (A ≈ 4 μm wide by 0.2 μm thick), normal metal resistivities (ρ_n ≈ 250 μΩ-cm for $YBa_2Cu_{2.8}Co_{0.2}O_7$ at 65K), and normal metal thicknesses (L ≈ 100 Å): $R_n = \rho_n L/A \approx 0.03\ \Omega$. It is apparent that SNS devices without significant interface resistance are unsuitable for SFQ applications. Note that inductance constraints make smaller devices undesirable, while higher resistivity N-layers would have shorter normal metal coherence lengths, ξ_n, and smaller I_cR_n products, aside from possible resonant tunneling effects [7].

Increasing SNS device resistances to a practical level requires the addition of interface resistance without significant degradation of the inherent I_cR_n product, which is possible through the incorporation of inhomogeneous interface resistance to reduce the effective device area [1] or by including a thin insulator at one SN interface to form an SINS structure. In practice different groups have seen widely varying values of SNS resistance, ranging from the ideal but impractical case of very low R_nA [2], to the more technologically interesting case of high-R_nA devices [1,6,7]. An open question has been why such diverse results are obtained with nominally similar SNS edge junction processes [1,2]. In an attempt to answer this question and gain some understanding of the nature of the interface resistance in SNS edge junctions, we examined some of the parameters which might affect SNS device resistance. We have discovered that a number of factors can dramatically increase SNS device resistances, while preserving SFQ-compatible I_cR_n products in many cases. These factors include the base electrode edge angle, the base electrode material, and the deposition parameters of the normal metal and counterelectrode.

II. Fabrication Details

Details of our SNS junction fabrication process have been described previously [1,3,4], but a brief summary will be given here. Base electrode YBCO films are deposited on $NdGaO_3$ substrates by off-axis sputtering or pulsed laser deposition (PLD). We typically use a CeO_2 or $SrTiO_3$ (STO) buffer layer with a CeO_2 or STO cap above the superconductor. Our PLD-deposited base electrodes are often La-doped, ($YBa_{2-x}La_xCu_3O_7$ with x=0.025-0.05) because we have found that a small amount of La can help suppress a-axis grain formation [3]. The base electrode edges are patterned using reflowed photoresist and 150 - 300 eV Ar ion milling at 45° with rotation. An Ar/O_2 mixture is sometimes used during milling to adjust the edge angle.

Although some groups have reported roughening of annealed YBCO edges under certain conditions [8],[9], we see no evidence for this effect with our own process. Fig. 1 shows an atomic force microscope (AFM) scan of a CeO_2/La-YBCO/STO-cap base electrode edge after

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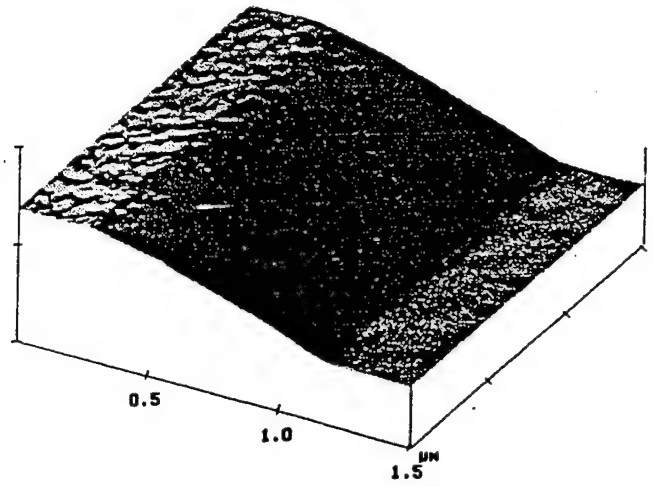

Fig. 1. AFM scan of La-YBCO base electrode edge after annealing at 805°C for 15 min. The RMS roughness on the edge is 8 Å. The vertical scale is 0.5 μm per div.

Ar ion mill patterning at 300 eV, followed by a 100 eV *in-situ* Ar ion cleaning step. The pictured edge was annealed at ≈ 805°C for 15 minutes in 400 mT O_2 to simulate the typical edge treatment just before normal metal and counterelectrode growth. The RMS roughness measured on the edge is approximately 8 Å both before and after annealing. AFM examination of a similar device edge following deposition of 100 Å of Co-doped YBCO shows only a slight increase in surface rougness to 9 Å. Possible differences between our process and those used by groups reporting rougher edges include our use of tapered resist milling masks with rotation during milling [9], and our lower temperature edge annealing [8].

Recently we have also investigated Br etching for edge cleaning [10]. The etching is typically done in a 0.3% Br in methanol solution for 10-30 sec. Initial results indicate that Br etching is an effective cleaning treatment. Following edge cleaning, the $Co_{0.2}$-YBCO and counterelectrode are deposited and patterned, and the devices are ready for bonding and testing.

III. RESULTS

A. *Factors Affecting SNS Device Resistance*

Because of the importance of high resistance SNS junctions for SFQ applications, we undertook a study of some of the parameters which could affect device resistance. Here we will concentrate on a number of factors that have a strong influence on SNS edge junction resistance including the base electrode edge angle, the base electrode material, and the deposition conditions of the normal metal and counterelectrode.

To study the effect of edge angle, we fabricated a series of SNS junctions on base electrodes with edge angles ranging from ≈ 12° to 36° (measured from the horizontal). These junctions showed a wide range of resistances and electrical behavior [3]. We observed that devices with relatively shallow edges (<15°) generally exhibited *void formation* in the counterelectrode (and possibly the normal metal layer) at the base electrode edges. This nonuniform edge growth is presumably due to a difference in surface mobility on the shallower edges. The shallowest-edge SNS junctions also showed "flux-flow" I-V characteristics and nonideal magnetic field modulation of the critical currents, consistent with inhomogeneous conduction through the devices. In addition, we found that the device resistances correlated with the base electrode edge angles, with R_nA products ranging from approximately 50 Ω-μm² for 11.5° edges to less than a few Ω-μm² for edge angles greater than 25°. The SNS junctions produced on steeper edges (>25°) also exhibited much more ideal electrical behavior, as will be seen below. The void formation, the magnetic field modulation data, and the high R_nA products associated with the shallow-edge devices are all consistent with a reduction in the effective area for these junctions, on a length scale not much less than the junction width.

We have also found that the base electrode material and deposition technique can have a strong effect on SNS device resistances, while the counterelectrode material does not have a significant influence. We see large differences in R_nA products for junctions fabricated with PLD YBCO, sputtered YBCO, and PLD La-doped YBCO base electrodes. Table I presents 77 K data for ion-mill-cleaned PLD $YBa_{1.95}La_{0.05}Cu_3O_7$ and PLD $YBa_2Cu_3O_7$ base electrodes with 30° edge angles, 50 Å $Co_{0.2}$-YBCO normal metal layers, and two different PLD growth conditions for the normal metal and counterelectrode. *For either growth condition we see more than an order of magnitude reduction in the R_nA product for the PLD-deposited YBCO base electrode*

TABLE I

R_nA AND J_c DEPENDENCE ON FABRICATION PARAMETERS

Base electrode	R_nA (Ω-μm²)	J_c(A/cm²)	N&C growth
PLD La-YBCO	4.56	≈ 2 x 10^2	Standard[a]
PLD YBCO	0.42	2.9 x 10^4	Standard[a]
PLD La-YBCO	0.76	4.4 x 10^3	800 mT O_2:Ar[b]
PLD YBCO	0.03	6.5 x 10^5	800 mT O_2:Ar[b]

Average SNS chip data at 77 K showing dependence of R_nA and J_c on base electrode material and the normal metal (N) and counterelectrode (C) growth conditions. The N-layers are 50 Å of Co-YBCO and all base electrodes have CeO_2 buffer and cap layers. Ion mill edge cleaning was used for all cases.

[a]Standard PLD N&C growth conditions are: N-layer - 805°C, 600 mT O_2; counterelectrode - 805°C, 400 mT O_2.

[b]The O_2:Ar ratio is 1:1.

relative to the La-YBCO base electrode, with an even larger associated increase in current density. Sputtered base electrodes typically exhibit R_nA products ≈ 0.3 - 0.7 times that of the PLD La-YBCO base electrodes. Preliminary results also show that coevaporated GdBCO and NdBCO base electrodes produce SNS devices with ≈ 3 - 5 times higher R_nA products than PLD La-YBCO, while coevaporated YBCO base electrodes give comparable R_nA products. *Overall, the PLD-deposited YBCO base electrodes consistently produce SNS edge junctions with the lowest R_nA products of any base electrode material.* Recent results using Br-edge cleaning show R_nA products reduced by a factor of 3-5 compared to in-situ ion mill cleaning. However, the relative difference in device resistances with PLD deposited La-YBCO and YBCO base electrode is still preserved.

Table I also illustrates the dramatic effect that the normal metal and counterelectrode growth can have on SNS device resistances. Previous work had suggested that using oxygen-argon gas mixtures during PLD could reduce the number of particles in YBCO films [11]. We discovered that high pressure O_2/Ar growth of the N-layer and counterelectrode resulted in a large reduction in R_nA and increase in J_c relative to our standard growth conditions of 600 mT O_2 for the N-layer and 400 mT O_2 for the counterelectrode. The lowest R_nA products are obtained for the combination of PLD YBCO base electrodes and 800 mT O_2:Ar normal metal and counterelectrode growth. In this case, R_nA = 0.03 Ω-μm², which is within a factor of ≈ two of the zero-interface-resistance limit. The small resistances seen in this case may be due in part to the better edge coverage we generally see for higher pressure deposition [3].

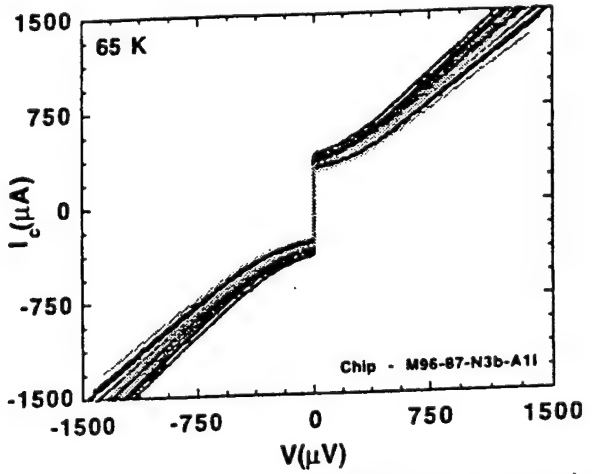

Fig. 2. I-V data at 65 K for a chip with junction parameters suitable for SFQ logic. There are nineteen 4-μm-wide junctions with 50Å Co-doped YBCO interlayers and an average resistance of 0.97 Ω (1-σ = 6%). The average I_c is 327 μA (1-σ = 13%) and the average I_cR_n product is 315 μV (1-σ = 9%).

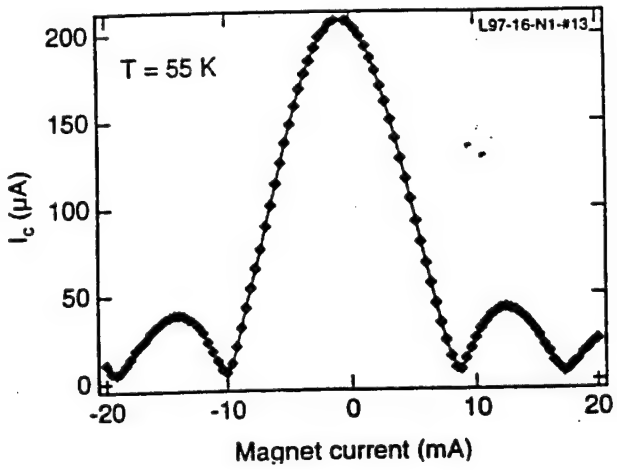

Fig.3. Critical current modulation at 55 K of a 4-μm wide SNS junction with La-YBCO base electrode with B normal to the substrate. The normal metal layer is 50 Å of Co-doped YBCO deposited after Br cleaning. At 55 K the junction resistance is 1.1 Ω.

B. SNS Current-Voltage Characteristics

SNS devices with edge angles greater than 25° almost always showed RSJ-like current-voltage characteristics. Fig. 2 shows the I-V characteristics at 65 K for nineteen 4-μm-wide SNS edge junctions with 50 Å Co-doped-YBCO normal metal layers. For this chip the base electrode YBCO-STO bilayer was sputter deposited, the edges were cleaned by Br etching, and the normal metal and counterelectrode were grown by PLD using the standard growth conditions described above. The average device parameters and spreads for these junctions were: $J_c = 4.1 \times 10^4$ A/cm², 1-σ = 13%; I_cR_n = 315 μV, 1-σ = 9%; and R_nA = 0.77 Ω-μm², 1-σ = 6%. The average values of critical current and resistance were 327 μA and 0.97 Ω. At 55 K, the J_c 1-σ spread for these junctions was 10%, and series arrays of 10 and 100 junctions fabricated on the same chip showed J_c 1-σ values of 6% and 10%, respectively. The combination of large resistances and I_cR_n products, tight J_c spreads, and small, SFQ-compatible critical currents is an important demonstration for the feasibility of HTS SFQ digital circuits.

The magnetic field modulation of the critical currents in these devices generally exhibits Fraunhofer-like behavior, as shown in Fig. 3 for the case of a typical high-R_nA SNS junction with a La-doped YBCO base electrode. The nearly ideal $I_c(B)$ modulation indicates that any nonuniformities in conduction are on a fine scale relative to the size of the junction. We have also investigated the temperature dependence of I_c and typically see the exponential temperature behavior expected for SNS proximity effect junctions. Curve fits to a standard proximity effect model give reasonable values of device parameters, even for high resistance

junctions[12,13]. For example, a proximity-effect fit for a device with a La-YBCO base electrode and a 75 Å $Co_{0.2}$-YBCO normal metal layer with $R_nA = 8.6 \times 10^{-9}$ Ω-cm^2 ($R_n = 0.96\ \Omega$) at 65 K gives $\xi_n(T_{cs}) \approx 26$ Å and $T_{cs} \approx 85$ K (where T_{cs} is the electrode transition temperature and T_{cn} is the normal metal transition temperature, which has been fixed at 45 K, consistent with independently measured values for $Co_{0.2}$-YBCO).

IV. Discussion

We have found that several factors have a significant effect on SNS edge junction resistance, including the base electrode edge angle, the base electrode material, and the deposition parameters of the normal metal and counterelectrode. We believe these factors are primarily affecting the interface resistances of the devices, rather than the "bulk" properties of the normal metal interlayer, because high resistivity N-layers would have shorter coherence lengths and smaller I_cR_n products (barring resonant tunneling effects). While adding interface resistance to an SNS device cannot increase the inherent I_cR_n product [12], reducing the active area of the device through an inhomogeneous interface resistance can increase the resistance without reducing I_cR_n [1] It is also possible to increase R_n without decreasing I_cR_n by fabricating an SINS structure with a thin deposited or naturally occuring insulator at one SN interface. Because the I_c value is fixed, approximately, by the requirements of HTS SFQ logic, adding interface resistance in these ways can increase the *practical* I_cR_n product—the value of I_cR_n available at that current level.

To date, the available data do not lead to a clear choice between the inhomogeneous or patchy interface model and the SINS model. The observation of edge voids for shallow-edge devices along with an associated increase in R_nA does suggest that a reduction in effective area is important in some cases. The temperature dependence of the critical currents demonstrates that even the high R_n devices are behaving as true proximity effect junctions, but this does not rule out the SINS model. It is important to note that, even if the resistance in these SNS junctions is dominated by a patchy interface resistance, the nearly ideal $I_c(B)$ modulation and the tight I_c spreads indicate that any active area inhomogeneity is on a fine scale relative to the size of the junctions.

The base-electrode-dependent interface resistance in these SNS edge junctions may be due to cation disorder at the base electrode interface. It is known that cation disorder, such as Y and Ba interchange in YBCO, can lead to suppression of T_c in the HTS materials and that cation disorder is more prevalent in superconductors with cations having similar ionic radii such as NdBCO [14,15]. Indeed we see the largest junction resistances for base electrodes with cations that are relatively close in size such as NdBCO, GdBCO, and La-doped YBCO where La may interchange more readily with Y than Ba can. We also speculate that YBCO base electrodes deposited by various techniques may have different amounts of cation disorder leading to the differences in junction resistance seen in these cases.

The order-of-magnitude difference we observe in SNS junction resistance for devices fabricated with La-YBCO versus PLD-deposited YBCO base electrodes (Table I), is consistent with the large difference in R_nA and I_cR_n products reported by our group and the group at Conductus. Our baseline process has used La-YBCO base electrodes to produce high resistance SNS edge junctions [1], while the standard Conductus SNS process utilized PLD-YBCO base electrodes to fabricate SNS devices with very small interface resistances, but also with correspondingly low I_cR_n products at SFQ-compatible I_c values [2].

Table I also indicates that the normal metal and counterelectrode growth conditions can play a major role in controlling SNS resistances. The dependence on growth parameters demonstrates that, in general, the excess SNS resistances are not determined entirely by a pre-existing surface layer on the base electrode edge. Both the epitaxial template (i.e. the base electrode surface) and the normal metal growth conditions can affect the initial stages of epitaxy. This suggests that for some conditions the interface resistance is dominated by defects in the normal metal microstructure "frozen in" during the initial stages of Co-YBCO epitaxial growth. Another point to note is that we are able to vary SNS interface resistances by orders of magnitude using materials with similar thermal expansion coefficients. This demonstrates that the effects of thermal expansion mismatch on interface resistance, while possibly important in some cases [16], can often be dominated by other factors.

The very high values of interface resistance we see in some cases also indicated that it might be possible to form useful weak links without any deposited normal metal. Indeed, preliminary investigations of this regime show that high quality weak links can be fabricated with La-YBCO base electrodes overlayed directly by a counterelectrode [17]. This approach requires no ion damage surface treatment [18,19], and the initial data shows I_c spreads and I_cR_n products comparable to our Co-YBCO SNS junctions and suitable for SFQ circuit fabrication.

In summary, we have shown that SNS device resistances are strongly affected by a number of factors, including the base electrode edge angle, the base electrode material, and the deposition parameters of the

normal metal and counterelectrode. The interface resistance is believed to be associated with cation disorder at the base electrode SN interface as well as with defects near that interface frozen in during overgrowth of the normal metal. By choosing the proper base electrode material and normal metal growth conditions, it is possible to fabricate high quality SNS edge junctions with a wide range of interface resistances ranging from almost no interface resistance to cases where the interface resistance is dominant. Importantly, even in the high resistance limit required for SFQ applications the SNS edge junctions still behave like true proximity effect devices with good $I_c(B)$ modulation and tight I_c spreads. We have used these devices to demonstrate small-scale (≈ 10 junctions) HTS SFQ circuits [20], and are currently working towards higher levels of integration.

ACKNOWLEDGEMENT

We would like to acknowledge the assistance of J. C. Brown, G. Faychak, G. Madia, D. Matuza, R. Nye, S. Pieseski, and J. Uphoff. We also acknowledge useful discussions with A. Kleinsasser and K. Delin.

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Materials Basis for a Six-Level Epitaxial HTS Digital Circuit Process

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Abstract — **We have developed a process for fabrication of HTS single-flux-quantum logic circuits based on edge SNS junctions which requires six epitaxial film layers and six mask levels. The process was successfully applied to fabrication of small-scale circuits (≤ 10 junctions). This paper examines the materials properties affecting the reproducibility of YBCO-based SNS junctions, the low inductance provided by an integrated YBCO ground plane, and electrical isolation by $SrTiO_3$ or Sr_2AlTaO_6 ground-plane and junction insulator layers. Some of the critical processing parameters identified by electrical measurements, TEM, SEM, and AFM were control of second-phase precipitates in YBCO, oxygen diffusion, Ar ion-milling parameters, and preparation of surfaces for subsequent high-temperature depositions.**

I. Introduction

Practical application of Single Flux Quantum (SFQ) logic circuits fabricated in High-T_c Superconductors (HTS) is limited at present by a low level of integration of Josephson junctions with sufficiently uniform characteristics. SFQ gates must have a low inductance, L, consistent with a quantum of flux, $LI_c \sim \Phi_o = 2$ mA-pH, and a Josephson critical current, I_c, on the order of 0.5 mA for thermal noise stability. Two approaches for achieving such low inductances are to use an integrated thin-film HTS groundplane or to use submicron lithography. We chose to follow the former approach in the process described here.

The requirements for junction reproducibility are shown in Fig. 1 following the discussion in [1]. Reproducibility is expressed as the standard deviation of Josephson critical currents, I_c. The calculation of junction count for a particular level of junction reproducibility assumes a Gaussian distribution of critical currents, and circuit component margins of 30%, which have been shown to be realistic in both simulations and LTS circuit measurements for SFQ circuits. Since there is always some chance with a Gaussian distribution that a junction's I_c will fall outside of circuit margins, circuit yield is expected to be < 100% even for small-scale circuits with low junction counts.

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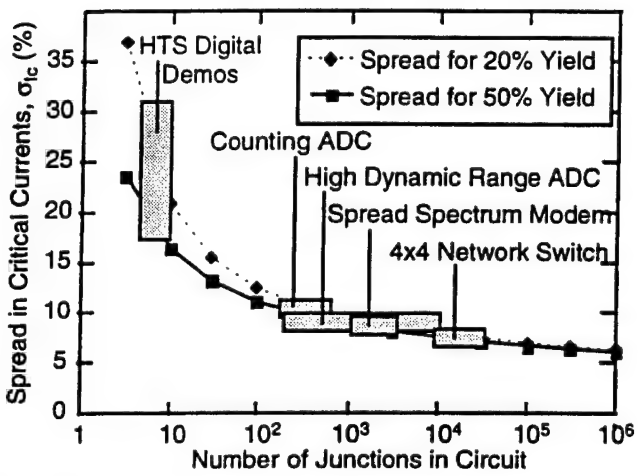

Fig. 1. The spread in junction critical currents, σ_{Ic}, required to produce circuits with a given junction count. Small-scale circuit demonstrations made to date are consistent with relatively large spreads in I_c of 20-30%. To fabricate SFQ circuits of practical interest with hundreds to thousands of junctions and reasonable yields, I_c spreads must be reduced to ≤ 10%.

Fig. 1 shows that one should expect no more than the small-scale SFQ circuit demonstrations made to date as long as σ_{Ic} = 20-30%. To fabricate circuits of practical interest with hundreds to thousands of junctions and reasonable yields, I_c spreads must be reduced to ≤ 10% while still satisfying the requirement for $LI_c \sim \Phi_o$.

Details are published elsewhere of junction electrical properties and some process issues [2-3], inductance measurements [4], and one of the circuits fabricated with this process [5]. The emphasis of this paper is in showing how the materials properties needed for groundplane integration and improved junction reproducibility are affected by the details of our integrated circuit fabrication process. Although the number of essential film layers is exactly the same, it is important to distinguish the multilayer film process for HTS digital circuits described here from that needed for integrating magnetometer pick-up coils with SQUIDs as in [6]. In the case of magnetometers, there is a minimal overlap of YBCO film layers which occurs only at crossovers. Junctions are fabricated directly on the substrate.

II. Integrated Circuit Fabrication Process

Major process steps we followed to integrate edge SNS junctions on an HTS groundplane are shown in Fig. 2. A minimum of six mask levels and six epitaxial oxide film

layers are needed for this process. Two additional epitaxial film layers were sometimes used, a 300 Å $SrTiO_3$ (STO) buffer layer between the substrate and groundplane, and a 300 Å STO cap layer deposited on top of the groundplane to protect the YBCO surface during processing. Since neither the presence or absence of these layers affected the sequence of process steps, we omitted them from the schematic cross sections of multilayers. Next we will describe in detail each of the six steps shown in Fig. 2.

A. Groundplane Deposition and Patterning

YBCO groundplane films 2250 Å thick were deposited by 90° off-axis rf magnetron sputtering with a process described in [7]. In all cases, $NdGaO_3$(110) substrates were used. In some cases, 2-inch diameter wafers were used which were diced into 1 cm × 1 cm chips at some point before circuit fabrication was completed so deposition parameters for the junction films could be varied while keeping groundplane fabrication parameters constant.

Fig. 3 shows the mask layout for (3a) a wafer, (3b) a chip, and (3c) a standard junction test subchip. The dark band on the subchip is the base electrode with two wire bond pads. The rest of the bonding pads are connected in pairs to the top electrodes of 20 devices. The edge SNS devices face in all four in-plane directions since this is a constraint imposed by the need for low-inductance connections in SFQ circuits. Junctions are spread out across each subchip to give a more complete measurement of junction uniformity.

Film patterning was done with photoresist masks reflowed for 5 min at 130°C. Wafers were tilted 50° from normal and rotated during 150 eV Ar ion milling to produce edges that angled 20-30° from the substrate plane. The same process was used to pattern single or multiple layers. SIMS endpoint detection prevented over-milling.

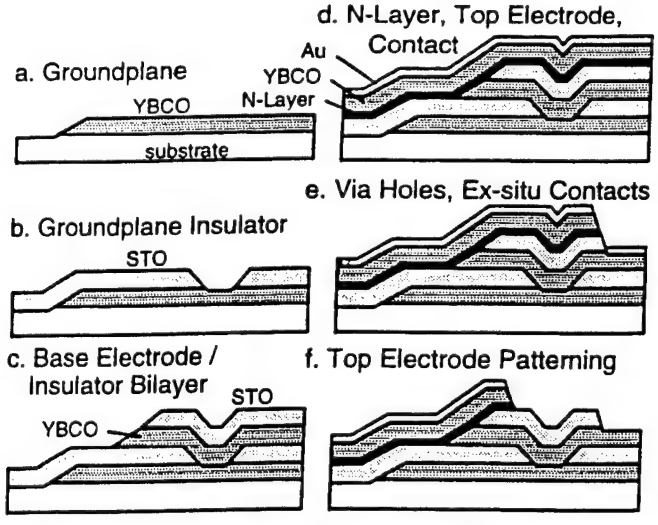

Fig. 2. The major process steps for fabrication of SFQ circuits with SNS junctions integrated on grounplanes for low inductance. The effect of each step on materials properties critical for groundplane integration and junction reproducibility are described in the text.

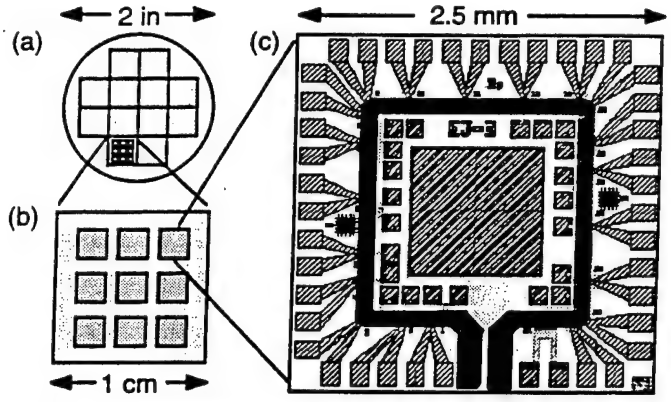

Fig. 3. YBCO groundplanes were deposited and patterned on 2-inch wafers (a) which were diced into 1 cm × 1 cm chips (b) for deposition of subsequent layers. Each chip had nine subchips where (c) was one of our standard patterns for measurement of twenty 3-μm-wide devices.

B. Groundplane Insulator Deposition and Patterning

Before we brought any patterned wafer up to ~700°C for deposition of a subsequent epitaxial layer, we cleaned the surface with an *ex-situ* oxygen plasma and a 150 eV Ar/O_2 ion mill to remove ~100 Å from the surface. XPS studies were used to ensure that hydrocarbon and fluorine residues were completely removed by the time the sample was brought to the desired deposition temperature [8].

Both $SrTiO_3$ and Sr_2AlTaO_6 (SAT) grown by off-axis sputtering were developed for epitaxial insulator films. Groundplane insulators were nominally 2400 Å thick but films used for insulator development varied in thickness between 1000 Å and 3000 Å without apparent thickness dependence. The important properties for the groundplane insulator were good electrical isolation and vias to ground capable of carrying currents greater than the junction critical currents (Fig. 2b).

A series of experiments were performed to determine which process parameters had the greatest effect on whether a minimum electrical isolation of 2×10^4 Ω-cm was achieved in YBCO/insulator/YBCO trilayer capacitors. We found that the insulator growth temperature in the range of 660-750°C, whether the layers were deposited without breaking vacuum, interfaces exposed to air, or interfaces exposed to ion-mill processing, were not significant factors. We also found that room temperature measurements were good predictors of isolation at 77K.

However, roughness of the first YBCO layer was found to be the key factor in determining electrical isolation. Fig. 4 shows the defect density in insulators inferred from the fraction of 35 capacitors per chip ranging in area from 1 mm × 1 mm to 250 μm × 250 μm. In [9], the defect density, D, is calculated from the "yield," the fraction of capacitors exceeding the minimum resistivity criterion, based on,

$$\text{yield} = (\#\ \text{working}) / (\#\ \text{tested}) = \exp(-D / \text{Area}) \qquad (1)$$

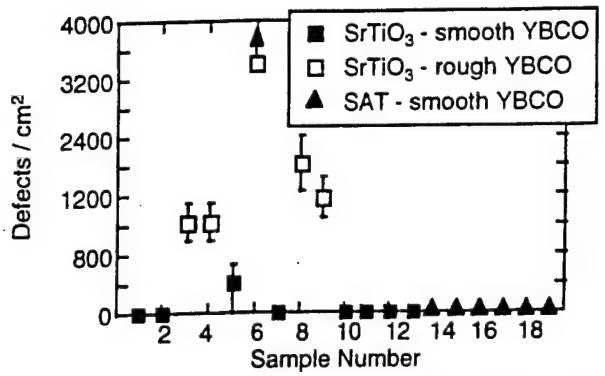

Fig. 4. Defect density for a series of 19 samples with 35 YBCO / SAT or STO / YBCO trilayer capacitors on each. Samples labeled as "smooth" had $\leq 10^3$ copper oxide precipitates per cm^2 in the lower YBCO film and, for all but one sample, no measured electrical defects.

Since we used two capacitors in series to measure yield, D was determined from,

$$\text{yield} = 1 - (1 - \exp(-D / \text{Area}))^2 \qquad (2)$$

The data in Fig. 4 are for a numbered series of samples with STO deposited on either rough or smooth YBCO base layers and SAT deposited on smooth YBCO. Error bars were based on potential changes in the yield by ±1 capacitor. For smooth films, only one leaky capacitor was found in 14 samples with a total of 490 capacitors. Nearly all of the capacitors exceeded the resistivity criterion by 4 or 5 orders of magnitude.

The definition of "rough" and "smooth" films in this case was based on the density of copper oxide precipitates which can be clearly seen, identified, and counted in an SEM. Smooth films had a density of $\leq 10^3/cm^2$ such "boulders," whereas rough films typically had 10^5-$10^6/cm^2$.

A cross-sectional TEM image of a YBCO edge SNS junction without a ground plane is shown in Fig. 5 to show the contrast between relatively smooth film layers, with rms roughness as low as 10-15 Å, and copper oxide boulders which disrupt insulator growth if they nucleate in one of the lower YBCO film layers.

Results of measurements of SAT and STO dielectric constants are shown in Figs. 6(a) and (b), respectively. Both data sets were independent of frequency in the measurement

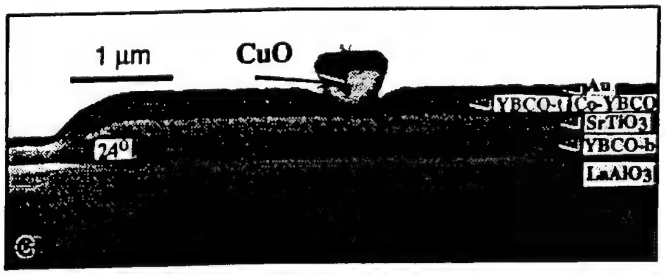

Fig. 5. Cross-sectional TEM image of an edge SNS junction without a ground plane showing the contrast between relatively smooth film layers and the potential for copper oxide "boulders" to disrupt multilayer structures. In this case, the boulder nucleated in the YBCO counterelectrode so it only disrupted the Au contact layer.

range up to 10 kHz. For SAT, $\varepsilon(77K) \equiv 26$ is in good agreement with SAT films grown by pulsed laser deposition [10], but is significantly higher than for bulk samples where $\varepsilon(90K) = 11.8$ [11]. For STO, $\varepsilon(300K)$ is in reasonable agreement with bulk samples but our STO films showed much less dependence on temperature than expected from bulk. Although we have made no direct measurements of dielectric loss, the anomalous behavior of STO films compared with bulk appears to be favorable since average voltage measurements of toggle flip-flips fabricated with STO groundplane and junction insulators indicated that they operated up to 15 GHz [12].

C. Base Electrode / Junction Insulator Formation

A YBCO base electrode 2250 Å thick and a junction insulator 1500 Å thick were sputter-deposited and patterned to form the structure shown in Fig. 2(c). The edge patterned at this step deserves special consideration since it formed one interface of SNS junctions. In addition to the *ex-situ* ion-mill cleaning described earlier, this edge was subjected to an *in-situ* 100 eV Ar ion mill to remove a few monolayers just before deposition of the normal-conducting, "N-layer."

D. N-Layer and Counterelectrode Processing

Results in [13] and [14] showed that the N-layer in SNS junctions which had the closest structural match to YBCO

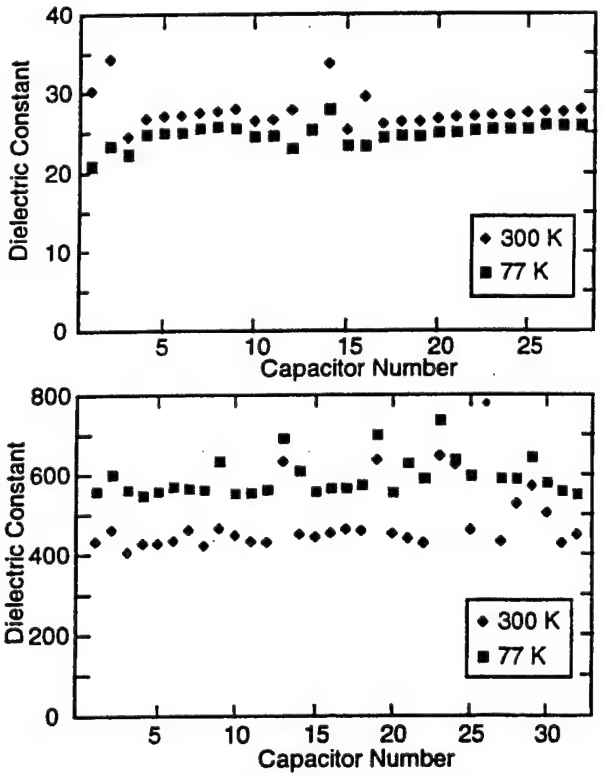

Fig. 6. Dielectric constants for (a) SAT and (b) STO epitaxial thin films deposited on YBCO. In comparison with bulk dielectrics, the most significant difference is the weak temperature dependence of STO.

led to junction characteristics which could best be explained by the standard model of proximity effects at S-N interfaces. Fig. 7 summarizes the dependence of junction critical current density, J_c, on N-layer thickness for three different N-layers based on doping YBCO with sufficient cobalt, calcium, and praseodymium, respectively, to reduce T_c to ~50K. For these N-layer evaluation experiments, we did not use a ground plane or rotate the samples during ion milling so all junction edges face the same direction.

Each data point in Fig. 7 represents the average J_c for all junctions on a chip and the error bars indicate the J_c spread. The normal-state coherence lengths, ξ_n(77K), calculated from the slope of the lines drawn in Fig. 7 are larger than expected from resistivites, ρ(77K), that varied from low values of 60-100 μΩ-cm for Ca-YBCO to high values of 300-600 μΩ-cm for Co-YBCO. However, the fact that J_c was an exponential function of N-layer thickness indicated that both edge formation and N-layer film growth on tapered edges were controlled processes.

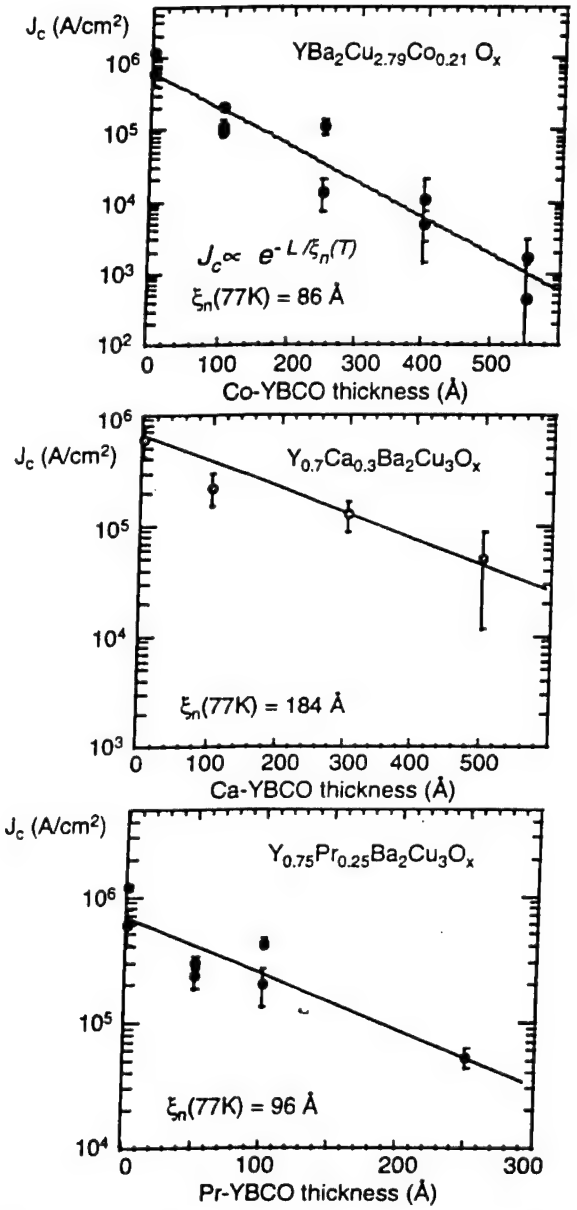

Fig. 7. Junction critical current density, J_c, plotted as a function of N-layer thickness for Co, Ca, and Pr-doped YBCO N-layers. Each data point represents the average J_c for all junctions on a chip and the error bars indicate the J_c spread. The exponential dependence of J_c on N-layer thickness shows the extent of our control over S-N interfaces and N-layer film growth.

High I_cR_n products for Co-YBCO junctions, 160-180 μV at 77K and ~500 μV at 65K, led us to focus on Co-YBCO. The Pr-YBCO junctions had I_cR_n products that were just marginally lower but I_cR_n for the Ca-YBCO junctions was a factor of 4 lower.

As shown schematically in Fig. 2(d), the selected N-layers, typically 75-200 Å thick, YBCO top electrodes 2000 Å thick, and 1000 Å Au contact layers were deposited sequentially without breaking vacuum. Although this process was originally developed using rf sputtering, indications of inhomogeneity in sputtered Co-YBCO encouraged us to fabricate junctions with N-layers, and necessarily, top YBCO electrodes, grown by pulsed laser deposition (PLD). Fig. 8 shows the differences in typical ρ(T) curves for sputtered and PLD Co(7%)-YBCO where the higher T_c, broader transition, and higher ρ(T) for the sputtered film were interpreted as signs of inhomogeneity. So far, the properties of our PLD junctions were not grossly different from sputtered junctions but the single chip with the tightest spread in I_c was fabricated with PLD.

E. Via Holes and Base Electrode Contacts

Fig. 2(e) shows the circuit structure after a via hole was ion milled to the YBCO base electrode and an *ex-situ* Au contact to the base electrode was patterned by lift-off. Via holes, crossovers, and step coverage were the subjects of a separate study of such passive structures for HTS digital circuits [8]. SEM micrographs of a test via and crossover are shown in Figs. 9(a) and (b), respectively. The most important characterization of these structures were

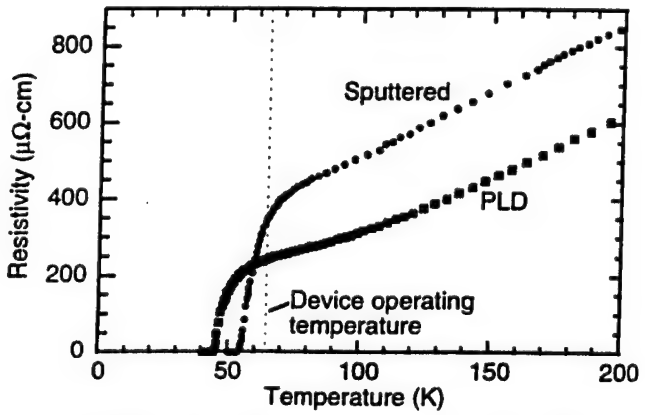

Fig. 8. Resistivity vs. temperature for typical Co-(7%)-YBCO films deposited by sputtering and PLD. Although sputtered films have resulted in junctions with desirable properties, their higher T_c, broader transition, and higher ρ(T) were interpreted as signs of inhomogeneity

measurements of electrical isolation (Fig. 4) and measurements of critical currents through vias and for films over steps. We designed vias in our circuits to have a large perimeter for contact compared to junction widths so they were never found to limit I_c. Fig. 10 shows that $J_c(T)$ for YBCO films covering 20 steps in either an STO underlayer or STO isolating YBCO cross-unders, was degraded by approximately one order of magnitude but could be kept larger than typical J_cs for either SEGB or SNS junctions.

F. Top Electrode Patterning

The last mask level was used to pattern the trilayer consisting of the N-layer, top YBCO electrode, and *in-situ* Au contact layer. Typical variations in the morphology of sputtered trilayers are shown in Fig. 11. Junctions for all three pictures had smooth base electrode films. In Fig. 11(a), both the Co-YBCO layer and YBCO top electrode were deposited at a low total sputter pressure of 125 mtorr. Under these conditions, it is relatively easy to avoid formation of copper oxide boulders and a-axis oriented YBCO outgrowths, and to obtain smooth surfaces on planar film regions. However, step coverage was poor as can be seen both in the junction area and in the rough pattern transferred by ion milling along the entire base electrode edge.

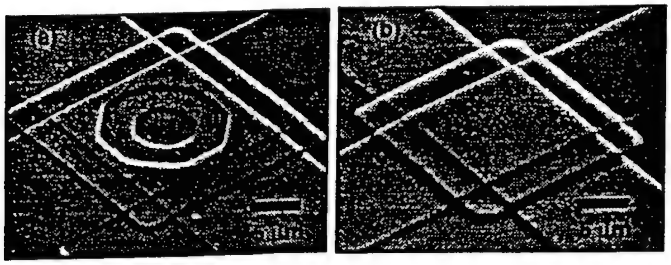

Fig. 9. Scanning electron micrographs of (a) a via hole and (b) a crossover test structure. These passive structures were characterized by measurements of electrical isolation as in Fig. 4, and J_c measurements as in Fig. 10.

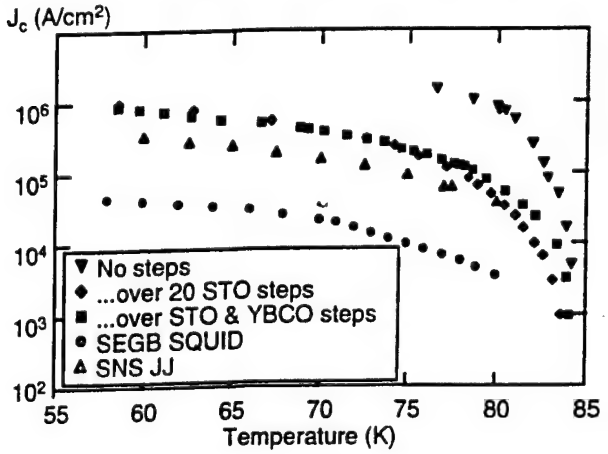

Fig. 10. Critical current density, $J_c(T)$, comparisons for YBCO films showing that coverage over multiple 20-30° steps degrades J_c by approximately an order of magnitude but not enough to cause a problem for SEGB or SNS-based circuits.

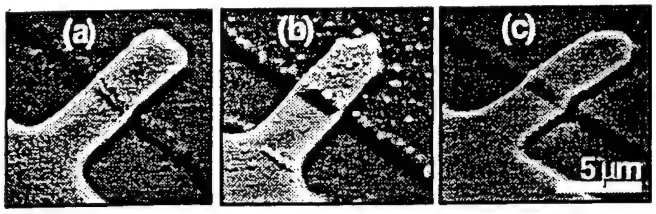

Fig. 11. Junctions 3 μm wide fabricated on smooth YBCO base electrodes. N-layers and YBCO top electrodes grown at low pressure (a) tended to exhibit poor step coverage whereas films grown at high pressure (b and c) were susceptible to boulder formation as in (b).

Figs. 11(b) and (c) show Co-YBCO and YBCO films deposited with the same Ar:O_2 ratio of 2:1 as in Fig. 11(a), but with a total pressure of 185 mtorr. In these cases, good step coverage was achieved but both the N-layer and top electrodes were susceptible to boulder formation. We believe that the difficulty in obtaining the film morphology shown in Fig. 11(c) was the greatest contributing factor to spread in junction critical currents.

A cross-sectional TEM micrograph of a junction without a ground plane is shown in Fig. 12. This sample had a 100 Å thick sputtered Co-YBCO N-layer (not distinguishable in the image) and a smooth edge as in Fig. 11(c). Simulations of phase contrast showed that the cobalt-doped layer could only be seen for a few select specimen thicknesses and defocus conditions. Nevertheless, it was observed that the bottom film was nearly free of defects up to the interface while the top electrode had stacking faults in the junction region.

III. Possible Origins of Junction Variability

Having established a baseline process for SNS junction and HTS digital circuit fabrication, we examined whether variations in the critical currents of junctions produced in this way were due to fluctuations in the parameters we controlled or due to intrinsic materials properties. In this section, we will present the results of experiments designed

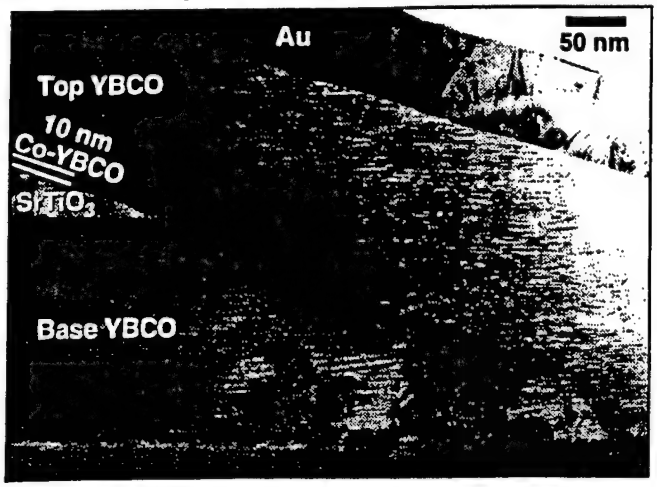

Fig. 12. Cross-sectional TEM micrograph of a junction with Co-YBCO N-layer and a smooth edge as in Fig. 11(c). Since the Co-doped layer could not be distinguished, the only visible defects are stacking faults in the top YBCO film in the vicinity of the junction.

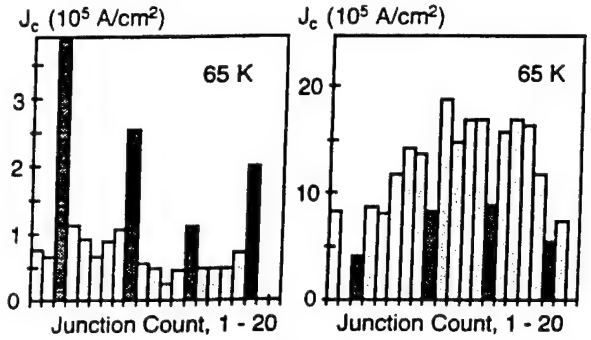

Fig. 13. Junction critical current density vs. junction number for two chips with Co-YBCO N-layers. YBCO <110> junctions (highlighted) tended to have different J_cs than <100> but not consistently larger or more uniform.

to test whether some intrinsic materials properties of YBCO were limiting junction reproducibility.

We always aligned photomasks so junction edges faced in YBCO <100> in-plane directions. However, some of our 20-device subchips (Fig. 3c) had 4 junctions with edges facing in <110> directions to test whether crystal anisotropy or twinning affected J_c uniformity. Fig. 13 shows J_c data for two such chips with the <110> data highlighted. Typically, YBCO <110> junctions tended to have different J_cs than <100> but not consistently larger or more uniform.

To test these ideas further, we fabricated junctions with $Y_{1-x}Ca_xBa_{2-x}La_xCu_3O_y$ (YCBLCO, x = 0.4) tetragonal electrodes. YCBLCO was shown to be highly resistant to corrosion [15], and we measured lower oxygen diffusion rates with in-furnace resistivity measurements at 400-500°C than in undoped YBCO films. I-V characteristics for 10 junctions on one chip fabricated with YCBLCO electrodes are shown in Fig. 14. Junction resistance tended to be high so I_cR_n at 65K was 500 μV even though the electrode T_c was just 78K. Junction I_c uniformity was poor over large areas because these initial sets of YCBLCO films had a 10^5/cm^2 density of CuO boulders.

IV. Conclusions

The YCBLCO experiment confirms the conclusion stated previously that the most important attribute for integration of junctions with groundplanes and for improved I_c uniformity is to produce smooth multilayer film surfaces. Small-scale circuits could be fabricated and demonstrated with our process because we have some control over this factor. However, experiments designed to determine intrinsic limits to I_c uniformity will not be definitive until this extrinsic factor is completely controlled.

Acknowledgment

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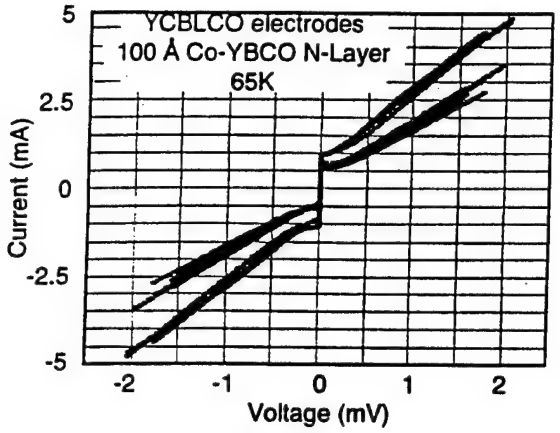

Fig. 14. I-V characteristics for 10 junctions fabricated with YCBLCO electrodes and Co-YBCO N-layers to test the effects of tetragonal structure and lower oxygen mobility.

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High-T_c SNS Edge Junctions with Integrated $YBa_2Cu_3O_x$ Groundplanes

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Abstract—**We have fabricated high-T_c SNS weak links in an edge geometry with integrated $YBa_2Cu_3O_x$ (YBCO) groundplanes and $SrTiO_3$ insulators, using a process which incorporates six epitaxial layers, including a Co-doped-YBCO normal-metal interlayer. The SNS edge junctions were produced using films deposited by both off-axis sputtering and pulsed laser deposition. These devices exhibit tight J_c spreads and high I_cR_n products in a current density regime well-suited for SFQ circuit fabrication. We also describe results on SNS junctions fabricated in a novel "slot" geometry, designed to reduce junction and interconnect inductances.**

I. Introduction

Single Flux Quantum (SFQ) logic offers the promise of 10 GHz operation coupled with microwatt power dissipation at the logic gate level. Realization of this potential requires the fabrication of high quality Josephson junctions in a multilevel epitaxial process. In particular, junctions with high critical-current - normal-state-resistance (I_cR_n) products (>200 μV), tight critical current spreads (<15%), and low junction and interconnect inductances are needed. The inductance constraints are most readily satisfied by incorporation of a superconducting groundplane.

We have recently reported on the fabrication of high performance SNS edge junctions and SQUIDs integrated with YBCO groundplanes[1], and good progress in this area has also been made by other groups[2], [3]. In this paper we discuss fresh aspects of the fabrication, including details of a new pulsed laser deposition process, alternate multilayer processing schemes, and recent results on the effect of edge angle variations on device properties. We also present new electrical data for SNS junctions with and without groundplanes with emphasis on devices with critical currents suitable for SFQ circuits. Finally we show results on a novel "slot junction" geometry, which enables the fabrication of lower inductance junctions and interconnects.

II. Process Details

A. Film Growth

The YBCO, $SrTiO_3$ (STO), and Co-doped YBCO (usually $YBa_2Cu_{2.8}Co_{0.2}O_x$), films used in this work were deposited by off-axis rf magnetron sputtering or by pulsed laser deposition (PLD). To date, sputtering has been used for deposition of every layer for some chips, and is always utilized for growth of the groundplane and groundplane-insulator, because the best sputtered films tend to be smoother than typical PLD films, which helps guarantee good electrical isolation between YBCO layers. Details of the sputter deposition were given in an earlier paper [1].

Our PLD film process has been primarily used for YBCO base electrode deposition and for completing junctions with growth of the normal metal and counterelectrode layers. Base electrode films were grown on STO buffer layers on $NdGaO_3$ (NGO) substrates. Typical YBCO deposition parameters were a nominal substrate block temperature of 805°C with a target-to-substrate distance of 5 cm, and an oxygen pressure of 400 mT. We were able to eliminate a-axis grain formation in the YBCO films by using targets with a small amount of La doping ($YBa_{1.95}La_{.05}Cu_3O_x$), a composition motivated by the possibility of obtaining higher T_c films [4]. La-doped YBCO films had T_c ≈ 87-91 K, and RMS roughnesses for 2000 Å films in a 10x10 μm AFM scan were ≈30-50 Å (this compares to ≈10-30 Å for the best sputtered films). Local smoothness of the PLD films was generally good (≈15 Å on a 2x2 μm scan), but scattered submicron outgrowths made the RMS roughness over larger areas somewhat worse.

The Co-doped YBCO films were grown under similar conditions except that the oxygen pressure was 600 mT. These deposition parameters produced films with the best electrical properties, but the 600 mT Co-YBCO films contained more outgrowths than for lower pressure growth. We found that the PLD-optimized $YBa_2Cu_{2.8}Co_{0.2}O_x$ thin films had electrical properties closer to bulk values than our best sputtered films: typical T_{cn} values were ≈45 K with 65 K resistivities of 250 μΩ-cm, compared to ≈55 K and 350 μΩ-cm for the sputtered films.

B. Multilayer Processes

1) Buried groundplane processes: Requirements for the fabrication of high performance multilayer circuits include the need for acceptable electrical isolation, high current density (J_c) vias and crossovers, high quality epitaxy of all layers, and complete oxidation of buried YBCO films. Details of the processing steps used to produce SNS edge junctions over buried groundplanes

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which meet these constraints were presented in [1]. In that work our multilayer process used two separate via patterning steps to make contact to the groundplane and to the base electrode. The result of this "double-via" approach is separate patterning and epitaxial overgrowth of the groundplane, the groundplane insulator, and the base electrode bilayer. Because epitaxial growth over a patterned film is quite sensitive to surface cleanliness of the underlayer, the yield of such a sequence of patterning and growth steps can be reduced, even with the cleaning procedure described in [1].

More recently we have also successfully produced edge junctions with groundplanes using a variation on this process in which a STO/YBCO-base-electrode/ STO trilayer is grown over the patterned groundplane as illustrated in Fig. 1. In this case contact between the base electrode and groundplane is made through large-area SNS junctions defined by a single via through the trilayer combined with counterelectrode "plugs" patterned at the same time as the junctions. The advantages of this "single-via" process are a reduced number of mask layers and *in-situ* growth of the base electrode trilayer, an inherently higher yield approach than the double-via process. Potential disadvantages are reduced circuit layout flexibility and lower-J_c via contacts. This approach is similar to a process first reported by Conductus [2]. At the present we are using both processes to produce junctions with groundplanes.

2) Groundplanes on top: Both the single and double-via processes are based on a buried groundplane configuration to minimize process exposure of completed SNS devices. However, it should be noted that there is no inherent reason to prohibit the use of groundplanes on top. Putting the groundplane above the junctions simplifies the processing, because groundplane morphology is no longer critical. In addition, fabricating the junctions directly on the substrate may ultimately lead to tighter device parameter spreads, and the groundplane and groundplane insulator serve as passivation layers for the buried junctions.

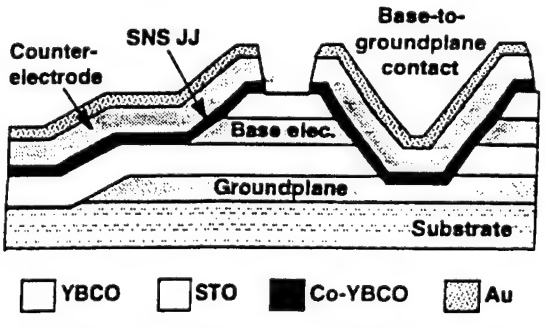

Fig. 1. Schematic cross section of a YBCO/Co-YBCO/YBCO SNS edge junction integrated with a YBCO groundplane in the "single-via' process. Contact between the groundplane and base electrode is provided by a counterelectrode plug.

We have begun experiments with groundplanes over SNS devices, with promising initial results. In this case we processed previously tested junctions without groundplanes by ion milling off the Au contacts, growing an STO layer, and patterning via contacts to the buried electrodes. Finally the YBCO groundplane was deposited and patterned, and Au contacts were defined. Results are discussed in Section III.

C. *Tapered Edge Effects*

Tapered base electrode edges with edge angles less than 45° are important for avoiding grain boundary formation in the counterelectrode[4]. Circuit layout considerations also make it desirable that the edge junction properties be independent of edge orientation. These constraints motivated the development of the reflowed-resist tapered edge process described in [1], which produced edge tapers of ≈30°. More recently, other results [5],[6] suggested that even shallower edges might be desirable. These reports led us to develop a modified tapered edge process utilizing an argon-oxygen gas mixture combined with the reflowed resist process reported earlier [1]. We found that milling at 300 eV in a 10% O_2 in Ar mixture at 45° produced 14° edges for lines of 20 μm or larger (all angles measured from the horizontal). Milling at 60° under these conditions produced tapered edges of 11.5°.

Our preliminary results with these shallower edge angles have revealed unexpected problems with *void formation* on edges below 15° in junctions completed by PLD at our normal counterelectrode deposition pressure of 400 mT. Higher pressure growth (up to 600 mT) improved the edge coverage, but resulted in increased CuO boulder formation. In the worst cases the voids were detectable in an optical microscope as an irregular edge, but AFM or SEM studies were needed to actually resolve the voids. Away from the device edges, film growth was uniform without holes. Sputtered SNS weak links showed better edge coverage over the shallow edges (at high deposition pressures), but both the PLD and sputtered devices exhibited nonideal electrical behavior, as discussed below.

III. Electrical Results and Discussion

A. *SNS Junctions Without Groundplanes*

1) Devices with shallow edge angles: PLD-completed devices fabricated on the 11.5 and 14° edges at growth pressures of 400-600 mT often exhibited "flux-flow" IV characteristics and nonideal magnetic field modulation of the critical currents, and tended to have degraded I_c spreads. In contrast, PLD devices on ≈30° edges showed excellent electrical behavior (next

section). These initial results also show that junction R_nA products correlate with the edge angles: R_nA products for three chips with 100 Å Co-YBCO interlayers and edge angles of 11.5°, 14°, and 30° were 51.5, 17.2, and 1.4 Ω-μm^2, respectively. While it is not surprising that junctions with voids at the edge exhibit higher resistances, these results *suggest* that the high R_nA products we observe even for the 30° edge devices [1] may be caused by nonuniform conduction associated with small voids along the edges.

Although the sputtered SNS devices had fewer obvious problems with edge coverage, they also tended to exhibit degraded junction quality and J_c spreads. The difficulties we observe with growth over shallow YBCO edges may be eliminated by further optimization of the growth conditions. However, our current efforts, described in the remainder of the paper, are focused on edge junctions with edge angles close to 30°, with which we can routinely produce high quality devices.

2) Devices with 30° edges: SFQ circuits require inductance (L) - Ic products on the order of a single flux quantum, $\phi_o \approx 2000$ pH-μA. Because typical microstrip inductances are about 1 pH/□ [1],[2], conventional SQUID layouts point to critical currents of a few hundred μA, with the lower limit set by thermal noise considerations. Fabricating devices with lower I_c values is accomplished by using thicker N-layers, which leads to an associated reduction in the I_cR_n products.

Fig. 2 shows the I-V characteristics at 65 K for nineteen 3-μm-wide SNS edge junctions without groundplanes with a 75 Å Co-doped-YBCO normal metal layer, which meet the SFQ critical current constraints (one junction of the twenty total on the test subchip was not measured due to a probe wiring problem). For this chip the base electrode YBCO-STO bilayer was sputter deposited and the normal metal and counterelectrode were grown by PLD. The average device parameters and spreads for these junctions were:

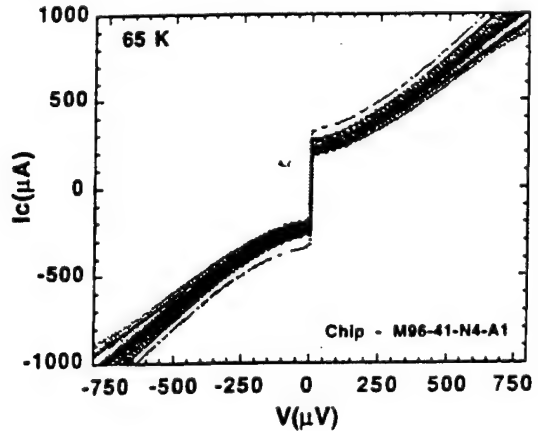

Fig. 2. I-V data at 65 K for nineteen 3-μm-wide junctions on a test chip without groundplanes with a 75 Å Co-doped YBCO interlayer. The 1-σ J_c spread is 16% and the average I_cR_n product is 181 μV.

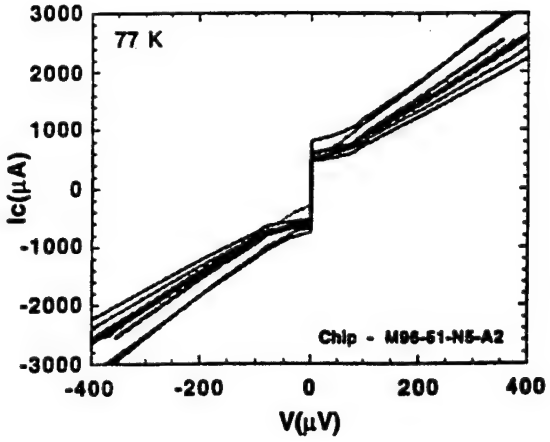

Fig. 3. I-V characteristics at 77 K for nine 4-μm-wide junctions with integrated groundplanes and 75 Å Co-YBCO interlayers. The 1-σ J_c spread is 16% and the average I_cR_n product is 100 μV.

$J_c = 5.0 \times 10^4$ A/cm^2, 1-σ = 16%; $I_cR_n = 181$ μV, 1-σ = 13%; and $R_nA = 3.7 \times 10^{-9}$ Ω-cm^2, 1-σ = 12%. The average values of critical current and resistance were 213μA and 0.82Ω. The current densities of these devices were lower than the J_c values of devices with sputtered Co-YBCO interlayers of similar thickness due to the different electrical properties of the sputtered and PLD Co-YBCO films. All but one of the devices exhibited nearly complete magnetic field modulation of the critical currents, with close to the expected |(sinx)/x| behavior. The combination of tight J_c spreads, large I_cR_n products, and small, SFQ-compatible critical currents seen on this chip is an important demonstration for the viability of HTS SFQ digital circuits.

B. SNS Junctions With Groundplanes

1) Buried groundplanes: The I-V characteristics for a recent set of nine 4-μm-wide SNS edge junctions over groundplanes are shown in Fig. 3. These junctions were fabricated using the double-via process with a sputterered groundplane and groundplane insulator, and a PLD base electrode, 75 Å Co-YBCO layer, and counterelectrode. In this case the test chip contained fewer individual junctions, but included other test structures such as SQUIDs and J_c bridges. At 77 K the average device parameters and spreads for these junctions were: $J_c = 7.5 \times 10^4$ A/cm^2, 1-σ = 16%; I_cR_n = 100 μV, 1-σ = 13%; and $R_nA = 1.3 \times 10^{-9}$ Ω-cm^2, 1-σ = 10%. At 65 K the average J_c increased to 2.9×10^5 A/cm^2 with a 1-σ spread of only 7%, demonstrating that very tight Jc spreads can be achieved over a groundplane, albeit with I_c values too large for SFQ applications in this case. These results also illustrate a trend seen for our recent groundplane chips: for a given N-layer thickness the average J_c has been higher and the average R_nA product lower relative to junctions without

groundplanes. This behavior was not seen in our earlier work [1], where junctions were very similar whether on or off of groundplanes. The more recent groundplane data may indicate that rougher growth in the upper layers of our multilevel structures is leading to device edge coverage problems, and, indeed, recent groundplane films have been somewhat rougher than in the previous work. These devices have proved suitable for fabrication of high quality SQUIDs and small-scale SFQ circuits [7],[8], and we expect that further improvements in the film process will lead to improved devices with reproducible characteristics both on and off of groundplanes.

1) Groundplanes on top: Two chips have been processed to add groundplanes over previously tested junctions as described in Section II. These devices exhibited RSJ I-V characteristics with very similar parameters to those before the groundplanes were added, *except* that the operating temperature of the junctions was reduced by about 20 degrees. At 50 K the average device values were: J_c = 1.8 x 10^5 A/cm^2; I_cR_n = 476 μV; and R_nA = 3.1 x 10^{-9} Ω-cm^2. This suggests that the high temperature insulator and YBCO growths done after junction fabrication led to oxygen depletion in the junction region, and we are investigating annealing procedures to re-oxygenate the devices.

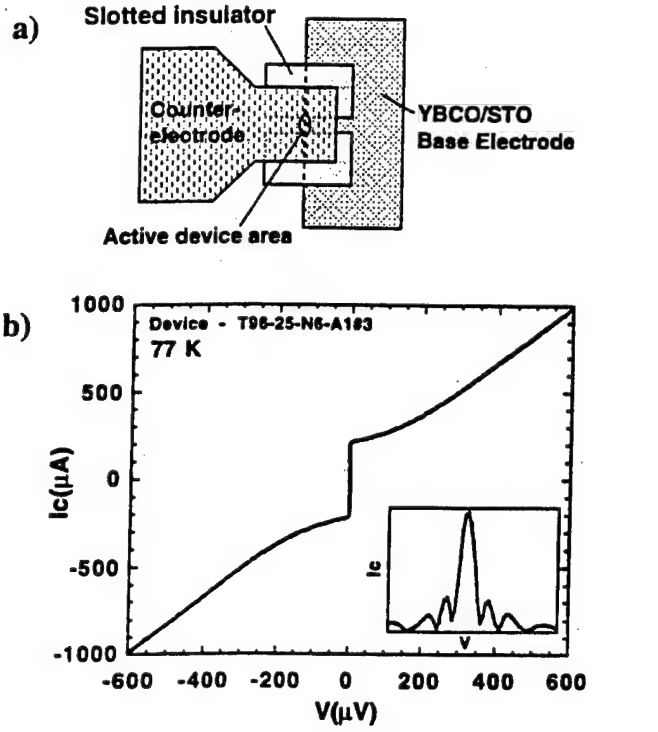

Fig. 4. a) Schematic diagram of slot-defined SNS edge junction. b) I-V and I_c(B) (inset) data for a sputtered slot junction with a 200 Å-YBCO normal metal layer at 77 K.

C. Slot-Defined SNS Edge Junctions

Obtaining SFQ-compatible LI_c products can be aided by patterning a slotted insulator layer over the SNS device edge as shown in Fig. 4a). This modification of the SNS edge junction geometry enables the use of wide, low-inductance counterelectrodes, while maintaining the small junction area needed for small-I_c, high R_n devices. The additional insulator layer also allows increased flexibility in circuit layout by enabling wiring to cross base electrode edges without shorting. In our initial experiments with the slot geometry, we patterned 3-μm wide slots in a 500 Å STO layer, combined with 10 μm-wide counterelectrodes. Fig. 4b) shows typical I-V and I_c(B) modulation data for a slot-junction device with no groundplane with a sputtered 200 Å Co-YBCO normal metal layer at 77 K. We have also fabricated slot-defined junctions and SQUIDs integrated with groundplanes, and SQUID measurements show the expected inductance reduction[7].

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ISTEC Hawaii '97

HIGH-RESISTANCE HTS EDGE S-N-S JUNCTIONS FOR DIGITAL CIRCUITS

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ABSTRACT

Current HTS circuit process development focuses mainly on SNS junctions, in contrast to the SIS junctions used in the more well-developed low temperature superconducting (LTS) technology. Despite the fact that S-N-S junctions have intrinsically low resistance we have found that it is possible to fabricate HTS S-N-S edge junctions with sufficiently high resistance for digital circuits (~ 1 Ω), and with critical current spreads as low as 10%, one-sigma. We argue that one significant factor in producing such high resistances is a reduction in the effective *area* of the junctions.

INTRODUCTION

Due to the difficulties inherent in fabricating S-I-S Josephson junctions based on HTS, a great deal of effort has been directed to developing S-N-S junctions, which have more relaxed materials requirements. In particular, edge (or ramp) geometry junctions, based on c-axis oriented YBCO films, have been the vehicle for exploration of a number of junction interlayers ("N-layers"). Our own efforts to develop HTS Single Flux Quantum (SFQ) digital circuits have emphasized the use of Co-doped YBCO. We, and colleagues at Conductus, have demonstrated the integration of these junctions with an HTS ground plane, producing the low inductance structures required for SFQ circuits [1-3], and we have used such a process to demonstrate simple HTS SFQ circuits incorporating up to ten junctions [4].

The use of Co-doped YBCO, and related materials, was motivated by the desire to minimize inhomogeneity at the S-N interfaces, which may be due to extrinsic effects such as etch damage, or to more intrinsic factors such as lattice-constant or thermal expansion mismatch, and which is thought to lead to lack of reproducibility and uniformity in junction parameters [5]. Since the doped YBCO N-layers are structurally well-matched to the YBCO electrodes the resulting junctions may be more ideal in that their resistance is dominated by the resistance of the N-layer material itself, rather than an interface resistance, and thus the junctions may be expected to be more reproducible.

In practice this approach leads to lower junction resistances ($\lesssim 0.1\ \Omega$) than is desirable for digital circuits (~ 1 Ω), however we have found that a number of fabrication parameters can have a large effect on the junction resistance, so that we can obtain a wide range of resistances while still achieving good reproducibility. While we do not yet understand the detailed mechanisms by which these fabrication parameters affect junction resistance, nor in fact what all the important parameters are, our data suggest that one important factor is changes in the effective area of the junctions.

JUNCTION FABRICATION

We have previously described the details of our junction fabrication process [1,6]. Briefly, films are deposited by either off-axis RF magnetron sputtering, at typical deposition temperatures of 780°C, or by on-axis pulsed laser deposition (PLD), typically at 805°C. The edge junction base electrode is capped by an epitaxial layer of either $SrTiO_3$ or CeO_2, and the

base electrode edges are etched with a 150eV-300eV Ar^+ source. An important aspect of the PLD process is that we sometimes use YBCO doped with a small amount of La ($YBa_{1.95}La_{0.05}Cu_3O_x$), which was initially chosen because it simplified the elimination of a-axis grains.

While several factors influence the junction resistance we focus here on three: base electrode material and deposition technique; normal layer deposition conditions; and base electrode edge angle.

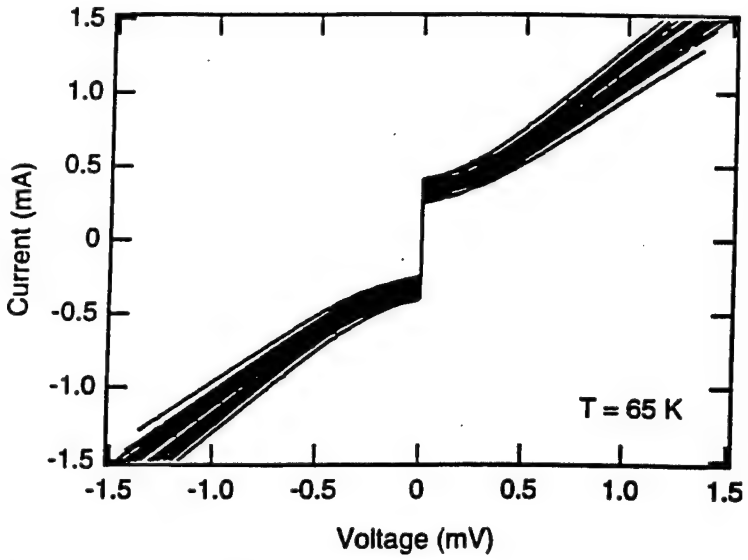

Fig. 1 – Current-Voltage characteristics for a set of 19 edge S-N-S junctions with parameters suitable for digital logic. Average parameters are: $J_c = 4.1\times10^4$ A/cm^2, $R_NA = 7.7\times10^{-9}$ Ω-cm^2, $R_N = 0.97$ Ω, $I_cR_N = 315$ μV, J_c spread (1-sigma) = 13%, R_n spreads (1-sigma) = 6%. The N-layer was 50Å of PLD-deposited $YBa_2Cu_{2.79}Co_{0.21}Ox$, and the base electrode 2000 Å of sputtered YBCO.

RESULTS

Effect of Base Electrode Material

Fig. 1 shows a set of current-voltage characteristics for a set of SFQ-compatible junctions utilizing sputtered YBCO base electrodes, exhibiting relatively narrow critical current spreads. Junction parameters are given in the caption. Of particular note is the average resistance, $R_N = 0.97$, which is about sixty times higher than the nominal resistance expected from the resistance of the N-layer itself, which, assuming our measured a-b resistivity of 250 μΩ-cm, is 0.016 Ω. In the case of PLD La-YBCO base electrodes we typically observe even higher resistances, sometimes as high as 100Ω, while PLD YBCO base electrodes typically lead to significantly lower resistance. Results for the dependence of R_NA on N-layer thickness, d_N, are shown in Fig. 2 for these three base electrode materials, where each data point represents an average over at least 18 junctions. Despite the scatter in the data it is apparent that the high junction resistances, in the case of PLD La-YBCO and sputtered YBCO base electrodes, are associated with a high effective resistivity, or a reduced effective area. According to conventional proximity effect models, such a high resistivity would lead to an extremely short normal metal coherence length, inconsistent with the observed magnitudes of critical current density. We therefore suggest that reduced area is the explanation. Also, for the two high resistance cases, it is fairly clear that the normal resistance is not dominated by a *series* resistance associated with the interface, since there is no significant vertical offset in R_NA versus d_N.

Effect of N-layer Deposition Conditions

For a given base electrode material we have found that a change in the deposition conditions of the normal layer can have a large effect on R_N and J_c. For example, for a PLD YBCO base electrode, increasing the deposition pressure from 400 mT to 800 mT led to a factor of ten reduction in junction resistance (and a factor of more than 100 increase in J_c) so that we obtained junction resistances as low as 0.03 Ω for a 50 Å Co-YBCO N-layer, which is only a factor of two higher than the expected intrinsic resistance. We have not yet studied this case in detail, since the resulting junctions have too low resistance to be useful for digital applica-

tions, but we suggest that the increased pressure typically leads to better coverage, in the case of the base electrode by the normal layer, and thus effective area more closely approaching the nominal junction area.

For the cases discussed so far we infer that the area inhomogeneity is on a length scale small compared to the nominal junctions dimensions, because the measured dependence of critical current on magnetic field, $I_c(B)$, is usually quite close to the behavior expected for a uniform junction. However, the fact that the minima in $I_c(B)$ are sometimes lifted above zero is consistent with nonuniform supercurrent conduction. The fact that we are able to observe critical current spreads as narrow as 10% (one-sigma) also argues against more gross area fluctuations.

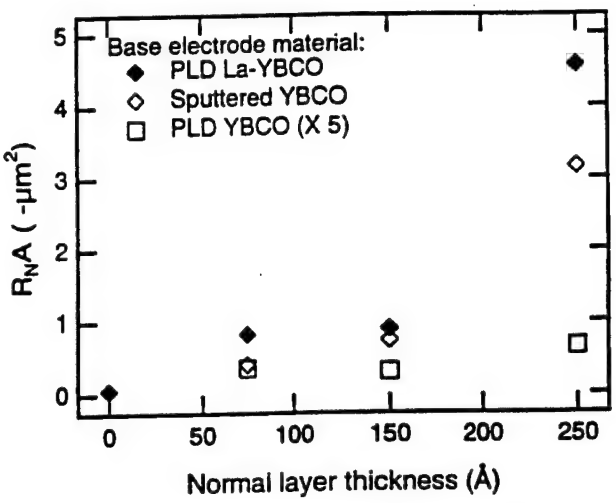

Fig. 2 – Junction resistance (times nominal junction area) versus N-layer thickness for three different base electrode materials, illustrating the broad range of resistances obtained. Data for PLD YBCO are multiplied by a factor of five to improve readability.

Effect of Base Electrode Edge Angle

For both of the above cases the inferred effective area reduction can not be directly observed by any of our readily available analytical techniques. However, when we fabricate base electrode edges with angles much less than our standard 20–30°, measured with respect to the substrate, we directly observe that *voids* form in the normal and/or counterelectrode films grown over this shallow edge. While the reasons for this poor growth are currently unknown the effects are readily measurable in the electrical characteristics of the resulting junctions. For example, $I_c(B)$ is no longer ideal, but rather is representative of a small number of parallel weak links. In addition, the junction resistance is considerably higher than for steeper (~30°) edges with better coverage, as illustrated in Fig. 3.

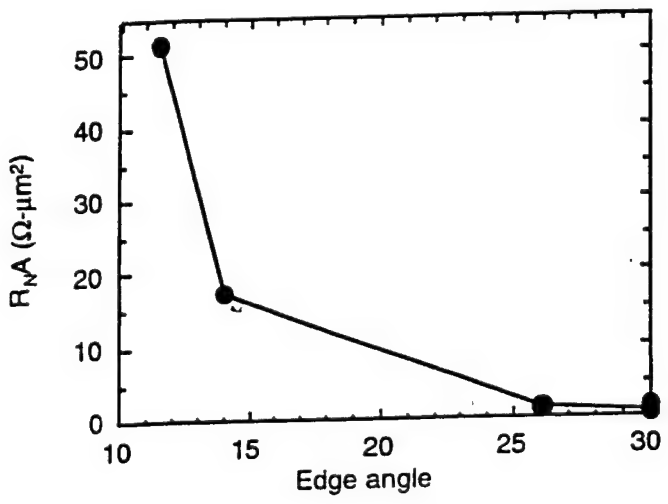

Fig. 3 – Junction resistance versus edge angle for PLD-deposited normal layer and counterelectrode. The increase in resistance is due to gross problems in coverage by the normal layer and/or counterelectrode.

DISCUSSION

We have argued that, for our HTS edge junctions, reduction in the effective area is at least partly responsible for the observed high junction resistances. This area inhomogeneity appears, in many cases, to be on a sufficiently fine length scale that the junctions behave relatively ideally in a magnetic field, and that relatively good critical current reproducibility is achievable. Further evidence that the

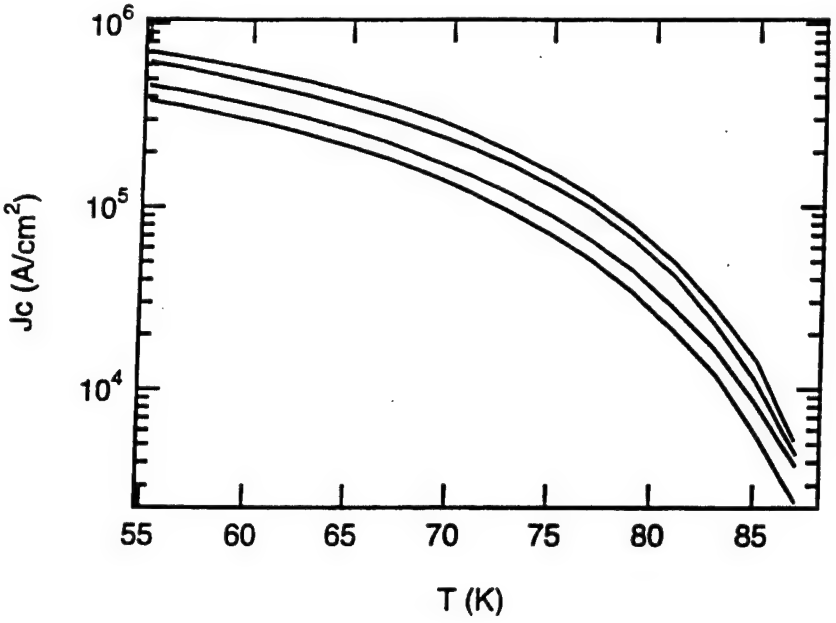

Fig. 4 – Critical current density versus temperature for four junctions on a chip. The curves differ mainly in their vertical displacement on a semi-log plot, consistent with effect area differences between the junctions.

measured I_c spreads are influenced strongly by area fluctuations is provided by the temperature dependence of $I_c(T)$ for different junctions on a chip. As shown in Fig. 4, we usually observe that semi-log plots of $I_c(T)$ show the data for different junctions to differ mainly in their vertical offset, which is consistent with different areas rather than, for example, different N-layer thicknesses or normal-metal coherence lengths.

We do not yet know whether this inhomogeneity, which may be different for quasiparticle- and supercurrents, will prevent us from obtaining the level of I_c control required for complex digital circuits, although we find the results to date quite encouraging.

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Appendix B: List of Project-Supported Presentations

The technical effort reported in these presentations was supported wholly or in part by USAF Contract No. F33615-93-C-5355.

1. J. Talvacchio, R. M. Young, M. G. Forrester, and B. D. Hunt, "Oxidation of Multilayer HTS Digital Circuits," Applied Superconductivity Conference, Palm Desert, September 1998.
2. L. R. Vale, R. H. Ono, J. Talvacchio, M.G. Forrester, B.D. Hunt, M. DiIorio, and K. Yang, "Stability of YBCO-Based Josephson Junctions," Applied Superconductivity Conference, Palm Desert, September 1998.
3. M. G. Forrester, B. D. Hunt, J. D. McCambridge, D. L. Miller, J. Talvacchio, R. M. Young, and J. X. Przybysz, "HTS Analog-to-Digital Converter Development," Applied Superconductivity Conference, Palm Desert, September 1998.
4. B. D. Hunt, M. G. Forrester, J. Talvacchio, and R. M. Young, "High-Resistance HTS Edge Junctions for Digital Circuits," Applied Superconductivity Conference, Palm Desert, September 1998.
5. J. Talvacchio, B. D. Hunt, M. G. Forrester, R. M. Young, A. S. Bhalla, L. E. Cross, S. Berkowitz, and K. Char, "Fabrication Technology for Josephson-Based HTS Digital Circuits," ONR Superconducting Electronics Workshop, China Lake CA, January 1998.
6. J. Talvacchio, B. D. Hunt, M. G. Forrester, B. D. Hunt, and R. M. Young, "Stability of Edge SNS Josephson Junctions," Materials Research Society Fall Meeting, Boston, November 1997.
7. B. D. Hunt, M. G. Forrester, J. Talvacchio, and R. M. Young, "High-T_c SNS Edge Junctions for Digital Circuit Applications," Workshop on Superconducting Digital Electronics, Winter Park, Colorado, September 1997.
8. M. G. Forrester, B. D. Hunt, J. Talvacchio, and R. M. Young, "High-Resistance HTS Junctions for Digital Circuits," 3rd ISTEC-MRS International Workshop on Superconductivity, Hawaii, June 1997.
9. B. D. Hunt, M. G. Forrester, J. Talvacchio, J. D. McCambridge, and R. M. Young, "High-Resistance SNS Edge Junctions," Intl. Superconductive Electronics Conf. (ISEC'97), Berlin, May 1997.
10. B. D. Hunt, M. G. Forrester, J. Talvacchio, J. D. McCambridge, and R. M. Young, "High-T_c SNS Edge Junctions for Digital Circuit Applications," in Proc. 9th International Symposium on Superconductivity - ISS'96, Sapporo,

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11. J. D. McCambridge, M. G. Forrester, D. L. Miller, J. X. Przybysz, B. D. Hunt, J. Talvacchio, and R. M. Young, "Multilayer HTS Counting A/D Converter," Applied Superconductivity Conference, Pittsburgh, August 1996.
12. B. D. Hunt, M. G. Forrester, J. Talvacchio, J. D. McCambridge, and R. M. Young, "High-T_c SNS Edge Junctions with Integrated YBCO Groundplanes," Applied Superconductivity Conference, Pittsburgh, August 1996.
13. M. G. Forrester, B. D. Hunt, J. D. McCambridge, D. L. Miller, J. X. Przybysz, J. Talvacchio, and R. M. Young, "Multilayer SQUIDs and SFQ Circuits Fabricated with HTS Step-Edge and Edge-SNS Junctions," Applied Superconductivity Conference, Pittsburgh, August 1996.
14. B. D. Hunt, M. G. Forrester, J. Talvacchio, J. D. McCambridge, and R. M. Young, "Transport in High-T_c SNS Edge Junctions," Workshop on Fundamental Processes of Electron Transport in High-T_c Junctions, Argonne, August 1996.
15. J. Talvacchio, M. G. Forrester, B. D. Hunt, J. D. McCambridge, and R. M. Young, "Six-Level Epitaxial Film Process for HTS Digital Circuits," Applied Superconductivity Conference, Pittsburgh, August 1996.
16. M. G. Forrester, B. D. Hunt, J. Talvacchio, J. D. McCambridge, R. M. Young, D. L. Miller, and J. X. Przybysz, "HTS Multilayer Process Development for Digital Circuits," in Proc. 4th NATO Workshop on Physics and Materials Science in High Temperature Superconductivity, Slovakia, July 1996.
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18. J. Talvacchio, M. G. Forrester, B. D. Hunt, J. D. McCambridge, and R. M. Young, "HTS Digital Integrated Circuit Fabrication," Materials Research Society Spring Meeting, San Francisco, April 1996.
19. M. G. Forrester, B. D. Hunt, J. D. McCambridge, J. Talvacchio, D. L. Miller, J. X. Przybysz, and R. M. Young,, "Inductance Measurements in Multilayer Edge- and Step-Edge SQUIDs," Materials Research Society Spring Meeting, San Francisco, April 1996.
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25. B. D. Hunt, M. G. Forrester, J. Talvacchio, and J. D. McCambridge, "High-Tc SNS Edge Junctions for SFQ Digital Circuit Applications," Workshop on Superconductive Electronics, Farmington, Pennsylvania, October, 1995.
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28. J. Talvacchio, M. G. Forrester, and J. R. Gavaler, "In-Situ High-Temperature Measurements of Oxygen Diffusion through Epitaxial Oxide Films," Materials Research Society Spring Meeting, San Francisco, April 1995.
29. J. Talvacchio, M. G. Forrester, D. L. Meier, and J. R. Gavaler, "Properties of Passive Structures for Multilayer HTS Digital Circuits," Applied Superconductivity Conference, Boston, October 1994.
30. M. G. Forrester, A. Davidson, J. Talvacchio, and J. R. Gavaler, "Multilayer HTS SQUIDs for Digital Circuit Applications," Applied Superconductivity Conference, Boston, October 1994.
31. M. G. Forester, J. Talvacchio, A. Davidson, and J. R. Gavaler, "HTS Junction Development at Westinghouse," ARPA HTS Josephson Junction Workshop, Washington, August 1994.
32. J. Talvacchio, "Applications of High-Tc Superconductors in Signal Processing," Ohio State University Nanostructure Materials and Devices Seminar, Columbus, May 1994.
33. J. Talvacchio, M. G. Forrester, J. R. Gavaler, D. L. Meier, and A. Davidson, "Ex-Situ Processing of Multi-Level HTS Structures," Materials Research Society Fall Meeting, Boston, November 1993.

Appendix C: Project Personnel

Principal Investigator (Northrop Grumman):	John Talvacchio
Principal Investigator (University of Cincinnati):	David Mast
Northrop Grumman scientists and engineers:	Martin G. Forrester
	Brian D. Hunt
	James D. McCambridge
	Robert M. Young
	Nathan Bluzer
	John R. Gavaler

Appendix D: Transport Properties of HTS Junction Arrays

This report was prepared by Prof. David Mast of the Department of Physics, University of Cincinnati, based on measurement of 2-dimensional junction arrays fabricated at Northrop Grumman.

Transport Properties of High T_c Ramp-edge Junction Arrays
University of Cincinnati

Our experimental efforts were focused on a wide variety of transport measurements on Northrop-Grumman's HTS superconductor- normal layer- superconductor (SNS) Josephson ramp-edge junction arrays. These measurements included a study of the low frequency noise, the resistive transition, the I_V characteristics and the single junction and array magneto-response. We investigated HTS square lattice arrays (both uniform and site-disordered arrays), hexagonal arrays and serial arrays. These arrays were fabricated from epitaxilly grown $YBa_2Cu_3O_{7-x}$ (YBCO) with a 3% Co doped YBCO normal layer. The arrays were developed and fabricated at the Northrop-Grumman Science and Technology Center (STC). Our major findings include the observation of anomalous low frequency noise in square lattice arrays, verification of filamentary conduction in the HTS junctions due to possible voids in the junction's normal metal layer, anomalous low field magneto-response behavior in hexagonal arrays and the first observation of vortex-anti-vortex creation and unbinding in site disordered square lattice arrays. A synopsis of our experimental results is given below describing 1). the transport measurements in square lattice, hexagonal and serial arrays, 2). the low frequency noise measurements in square lattice and serial arrays, and finally 3). the transport measurements for the site disordered arrays.

Transport Measurements in Square, Hexagonal and Serial Arrays

In looking at the transport properties of junction arrays, it is important to be able to separate single junction effects from array effects from geometrical effects. In part, this is important because as the global phase coherence of the system is weakened, due to increasing

temperature or bias current, sections comprised of one or more junctions will probably behave differently. In addition, differences in array geometry and junction parameters such as electrode shape between the square lattice arrays, hexagonal array and serial arrays, make direct comparison of transport data more complex and furthermore complicates the extraction of I_c and R for these arrays. In the case of normal state resistance, R, this difference could be accounted for, to a high degree of precision, by taking into account the known differences in electrode and counter-electrode size and shape. However, in the case of magnetic field response, where non-linear effects such as flux-focusing come into play, a quantitative comparison becomes more difficult. This is handled by comparing ratios of feature size, such as R or $V(B_z)$ to the total signal.

The resistive transition for square 9x9 arrays shows several distinct sections, see Figure 1. At the highest temperatures the curve is approximately linear with a resistance of 8.7 Ω at 96 Kelvin. As the temperature is reduced the resistance begins to drop more sharply with the first "knee" occurring around 91.6 Kelvin. At approximately 88.0 Kelvin there is a second knee where the drop in resistance begins a steeper drop before entering the "tail" section at around 87.0 Kelvin. This tail slowly approaches, but does not reach, zero resistance as the temperature is lowered and coupling energy of the junction increases. This portion of the transition has a strong magnetic field dependence and low frequency noise response as discussed below.

Of particular interest is the reason why the electrode and counter electrode have different superconducting transition temperatures. Because the electrode layer of YBCO is grown first and then covered by a STO insulating layer in preparation for etching of the ramp edge, we believe that degradation due to exposure to oxidizing agents or damage caused by processing of the counter electrode layer is unavoidable and responsible for these features. T_c measurements made

on bulk YBCO films show a T_c around 91.5 K, which is in agreement with the onset of the observed superconducting transition.

The calculated junction resistance based on width, thickness and resistivity equals 0.045 Ω. The calculation includes a value of the Co-doped YBCO normal layer resistivity equal to 295 μΩ-cm at 96 K. This result for the junction resistance, however, is considerably lower than the value of 0.87 Ω extracted from IV characteristics shown in Figure 2. [The dynamic resistance (dV/dI) rises sharply but smoothly from the low resistance state to a peak, at I_c, and then diminishes toward the junction normal state resistance as shown in Figure 3.] This indicates that the resistivity of the Co-doped YBCO present in this array is an order of magnitude higher than that of other Co-doped YBCO films produced by the Northrop-Grumman group, or that the effective junction area is considerably smaller than the simple geometrical cross section. A correlation between junction edge angle and degraded junction characteristics such as R_nA (A = junction area) products and the spread in I_c has also been observed by the Northrop-Grumman group. Measurements they made on junctions fabricated with edge angles of 11.5°, 14° and 30° showed R_nA products of 51.5, 17.2 and 1.4 Ω-μm^2. The increased R_nA products at the shallowest edge angles is attributed to incomplete edge coverage resulting in small voids along the electrode/normal YBCO and counter electrode/normal YBCO interfaces. These voids result in an increased R_nA product and nonuniform conduction path. This suggests that the large junction R_n value which is observed is due to irregularities along the ramp edge.

This latter hypothesis is also believed to the be correct for the following reason. For a junction of area A, the critical current of the junction should vary with magnetic field B (perpendicular to this area), as[1] a Fronhoffer type response in the applied flux / ϕ_o flux quanta.

For an array of junctions with voids or other non-uniformities along each junction face, the total $I_c(B)$ response will be an envelope consisting of a sum of the individual responses. This sum response will show a broadening of each peak and incomplete modulation, in addition to irregularities and some degree of broken symmetry. This is what has been observed as shown in Figures 4 and 5.

In contrast to the data for square lattice arrays, linear arrays display a considerably sharper resistive transition both in the upper knee and in the lower tail region, indicative of single junction like behavior: see Figures 6 and 7. However, unlike 2D arrays, there exist several discernable peaks in the dynamic resistance which correspond to individual junctions, or groups of several junctions, entering the voltage state at different current values as shown in Figure 8. By examining the difference in resistance between peaks, all ten junctions can be accounted for and this allows for the determination of the spread in I_c. We measure a spread in the critical current of individual junctions within the linear array from 0.76 to 1.33 mA, resulting in a standard deviation, σ, equal to 23%. This degree of deviation is similar to that of single 3 μm wide junctions fabricated and characterized by the Northrop group. In addition, we observe evidence of a linear tail in the I_V characteristics indicative of a resistive shunt in the linear arrays: see Figure 9.

The central tip of the magneto-response data is much broader and the degree of modulation considerably less complete than that of the 2D array as shown in Figure 10. This incompleteness of modulation is not unexpected given that the spread in I_c is 23%.

The hexagonal lattice array is made up of 1.5 μm wide junctions arranged in hexagonal plaquettes 8 μm on a side. Unit cells of the array are made up of Y-shaped electrodes with 4 μm

wide arms and Y-shaped counter electrodes with 1.5 μm wide arms. There are three junctions in each unit cell. In the direction of the applied current, the junction at the base of each Y is in series with the two junctions at the top of each Y. The current passing through the base junction must equal the sum of the currents in the two upper arm junctions.

In an array of identical junctions, the current in the base junction will split equally between the two upper arm junctions. As the bias current is increased, the base junction of each cell will enter the non-linear transition regime before the two upper arm junctions. As the current increases further and the base junction nears and passes its dynamic resistance peak, the upper arm junctions are just entering the non-linear regime. Finally, as the dynamic resistance of the base junction drops toward its normal resistance value, the upper-arm junctions are passing through their dynamic resistance peak. Because the base and upper-arm junctions are in series, the observed transition is a superposition of the base junction transition and upper-arm junction transition. Thus, the non-linear transition region occurs over a broader range of current in hexagonal array than in square lattice: see Figure 11. In addition, the resistive transition in zero magnetic field of an hexagonal array shows several distinct regions that correspond to these two" types" of junctions: refer to Figures 12 and 13.

There is a large degree of symmetry in the Fronhoffer magneto-response of the hexagonal arrays. The secondary lobes are better developed than those observed for square lattice arrays, although the central minimum is less pronounced as shown in Figures 14 and 15.

However, examination of the magneto-response of hexagonal arrays near $B_z = 0$ fails to show an observable response as a function of array frustration f. The reason for this is quite puzzling and is not known at this time. [Magneto-oscillations have been observed in hexagonal

LTS SNS junction arrays.] We are presently investigating whether this lack of magneto-oscillation (as observed in the square lattice arrays) is possibly related to the pairing state symmetry of the underlying HTS films, In the hexagonal array, the junctions that make up the upper part of the Y are at a 60° (30°) with respect to the *a* (*b*) crystallographic axes, while the junction that make up the tail of the Y are along (or perpendicular) to the *a* (*b*) axes. This difference could dramatically effect the ability of the array to form a commensurate flux lattice.

The results of these experiments are currently be written up for publication.

Low Frequency Noise Measurements

Noise measurements were made on 9x9 square lattice array and 10 junction serial array at frequencies below 50 Hz.. These measurements were motivated by numerical studies[2,3,4] and recent experimental studies[5,6,7] which report anomalously low vortex mobilities in Josephson junction arrays. These sluggish vortex mobilities are in conflict with expected values based on the Drude model of a two dimensional gas of free vortices[8]. As described by this model, the conductivity of free and independent vortices is proportional to the vortex density and independent of frequency[9,10] . This yields a characteristic time scale for free vortex diffusion of less than 10^{-5} seconds; a characteristic time value which is not in agreement with the noise voltage measurements described

The power spectral density (PSD) of the noise voltage across a 9x9 array, taken in zero magnetic field, shows a pronounced peak around 86K as shown in Figure 16. It is interesting to note that no difference in the PSD was observed even when the bias current was reduced to zero. This suggests that the mechanism responsible for these noise spectra does not correlate with a

macroscopic current. In particular, if vortex dynamics are responsible for the observed levels of noise voltage, they are not due to a macroscopic Lorentz force. Comparing the PSD response to the resistive transition, it is apparent that peak activity in the observed PSD response corresponds to the foot region of the resistive transition. In this region, phase coherence across the junctions is established as the temperature is reduced below 87 Kelvin and thermally assisted flux-flow resistance is believed to be responsible for the behavior which is observed.

In contrast to the increased PSD activity shown by a square array, the PSD response of a 10 junction serial array is nearly flat over the same frequency range, and shows no significant temperature dependence: see Figure 17.

The striking difference between the response of serial array and 9x9 array, in this frequency range, suggests that vortex dynamics are responsible for the observed difference.

To probe this hypothesis, the PSD of a 9x9 array was measured at values of transverse magnetic field corresponding to values of array frustration, f, equal to 0, 1/2 and 1. As the applied magnetic field is increased from an integer value of f to an irrational value of f, the DC voltage increases as the vortex lattice becomes increasingly incommensurate with the junction lattice. In these arrays, a local maximum in the DC voltage is observed at $f = 1/2$ and the voltage begins to decrease as f approaches 1: see Figure 18.

The PSD's at f = 0 and f = 1 are similar in amplitude and form. However, the PSD at $f = 1/2$ is suppressed by about approximately 40% between 0.625 and 10 Hz. Suppression of the noise voltage at $f = 1/2$is possibly caused by an increase in the pinning energy which a vortex lattice is known to experience when the array is frustrated at $f = 1/2$[11].

The present level of understanding of the anomalously slow vortex behavior implied by

this data precludes a clear description of the microscopic mechanism which is responsible. However, several possible explanations have been suggested, all of which warrant further investigation. Diffusion in disordered systems and systems with finite size effects has not been found to agree with classical predictions and these systems can exhibit anomalous transport properties.[12,13,14] Coupling of vortices with spin-wave excitations present in an array has been studied numerically and has been proposed as a source of low frequency dissipation in a 2D superconducting system.[15] Calculations of dynamic impedance made using Mori's formalism for a screened Coulomb gas[16] suggests that vortex pairs experience a velocity-dependent viscosity coefficient which decreases with increasing velocity. This leads to a prediction of sluggish (not Drude-like) vortex mobility at low frequencies.[17]

The preliminary investigation of low frequency noise voltage described in this section suggests that further temperature and magnetic field studies be made. In particular, a study of noise voltage in arrays with different pinning energies and different numbers of junctions. This might be accomplished by comparing noise spectra from square lattice and triangular lattice arrays or studying spectra from square lattice arrays of various sizes and aspect ratios, such that the effect of edge pinning is varied. Additionally, a study of bias current dependence would help to build a clearer understanding of the nature this low frequency behavior. The results of these experiments are also being written up for publication.

Site-disordered Square Lattice Arrays

In the site disordered 9x9 arrays, there are two large and two small defects which are located symmetrically about a diagonal connecting the upper-left and lower-right corners as

shown in Figure 19. The two large defects are identical in size, as are the two small defects. In the direction of the macroscopic current, there are six rows with two junctions missing and two rows with four junctions missing.

These disordered arrays show discernable structure between the knee and the low voltage ohmic region, due to the redistribution of current (ie. vortices) around the vacancies: see Figure 20. As the current density increases, vortices form and de-pin in a cascading sequence first from the defects and then from adjacent plaquettes. These de-pinned vortices cause voltage drops as they are driven across the array by the Lorentz force as shown in Figure 21. These are the first observations of vortex formation and unbinding in site disordered arrays. We are extending these measurements to include observation of the high frequency response of these site disordered and are investigating the potential of using such arrays as infrared detectors. These results will be published once the high frequency measurements are completed.

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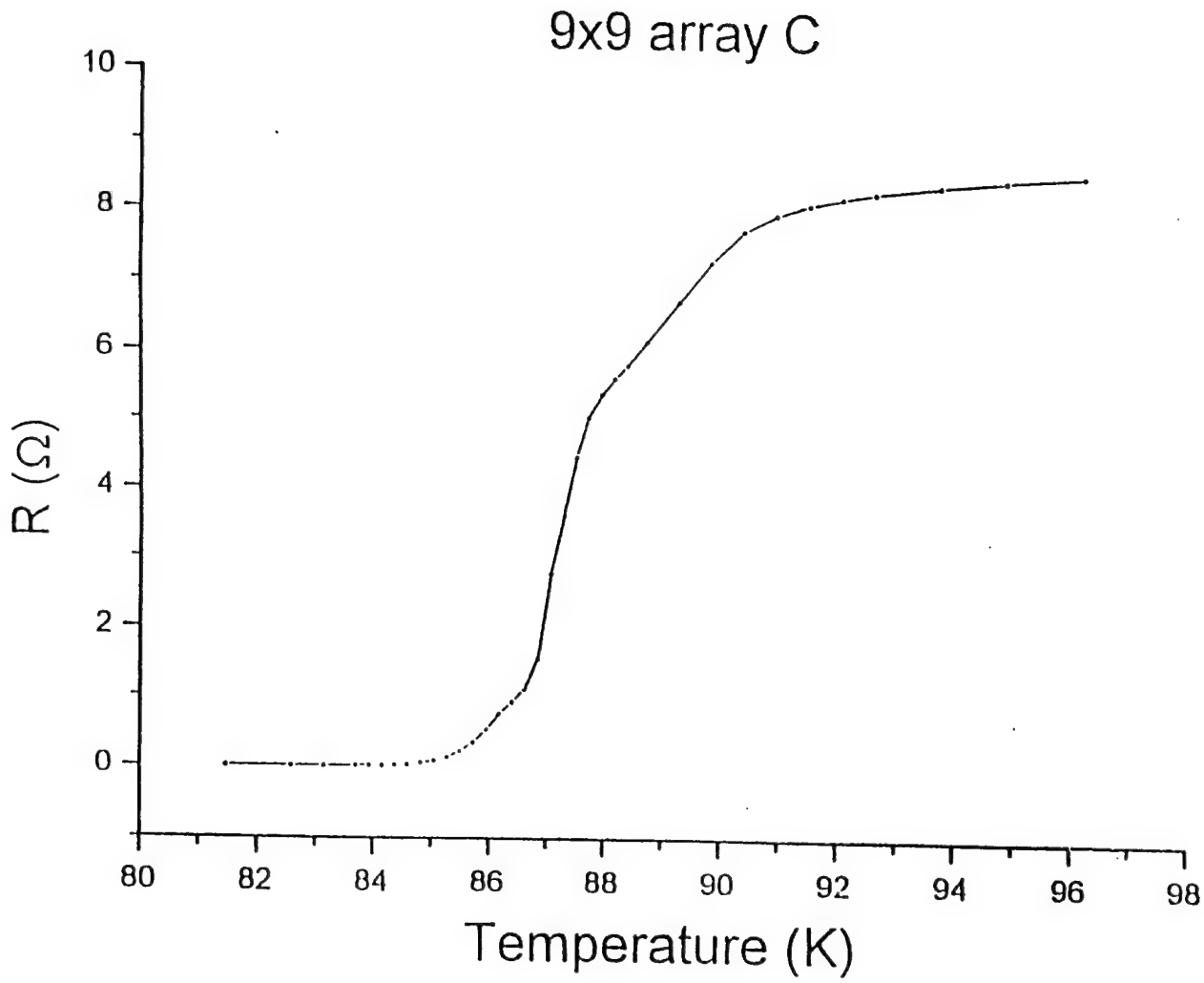

Figure 1 Resistive transition in zero magnetic field for 9x9 square lattice array C. The measuring current equals 1 μA.

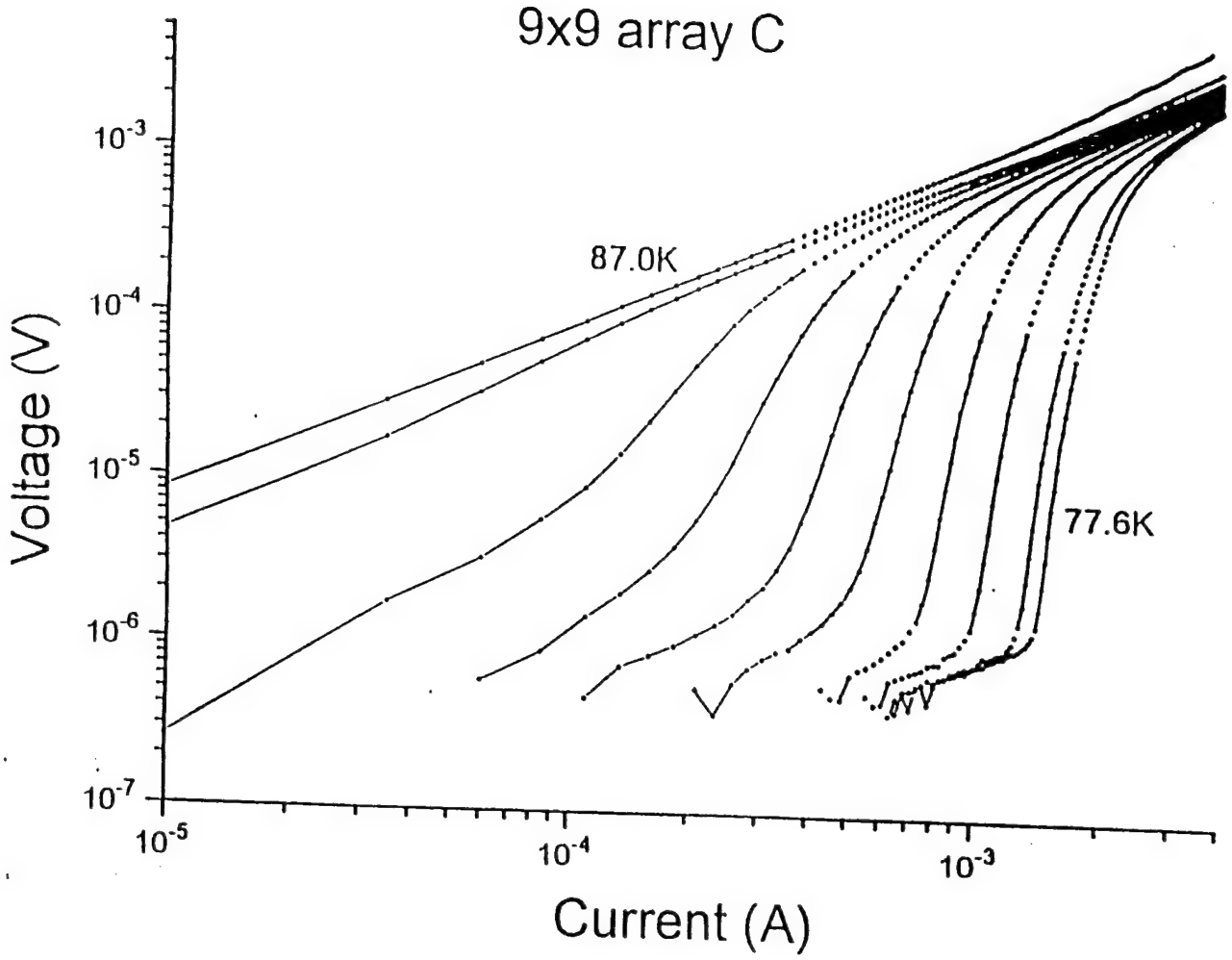

Figure 2 Log-log plot of IV curves for 9x9 array C. Temperatures shown are 77.6, 78.6, 79.7, 80.7, 81.8, 82.8, 83.9, 84.9, 85.9 and 87.0 Kelvin. Note the departure of the slope from one for large currents at the highest temperatures.

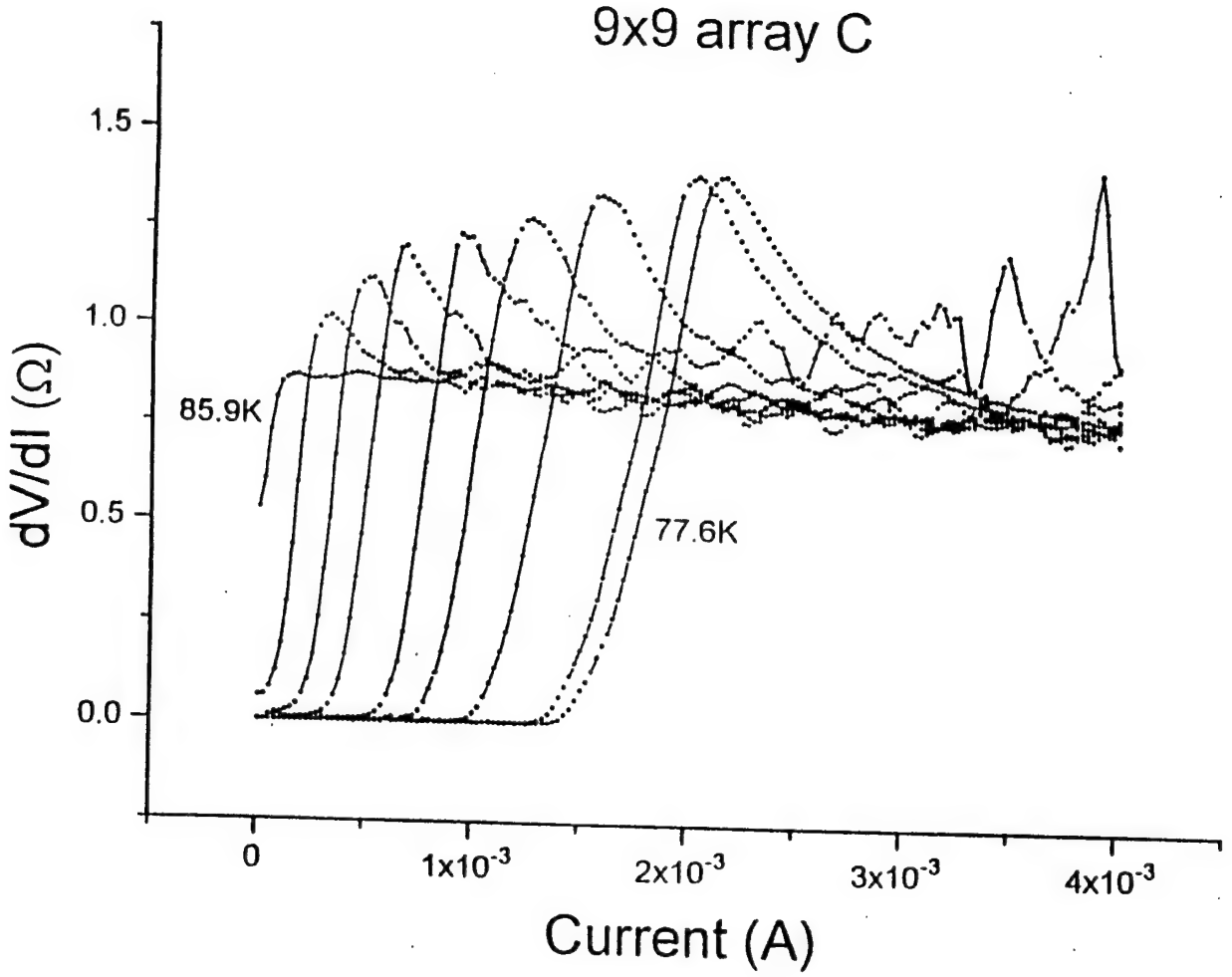

Figure 3 Plot of dV/dI taken from the curves shown in figure 2 Temperatures shown are 77.6, 78.6, 79.7, 80.7, 81.8, 82.8, 83.9, 84.9 and 85.9 Kelvin. Note the increasing instability due to temperature fluctuations for large currents at the highest temperatures.

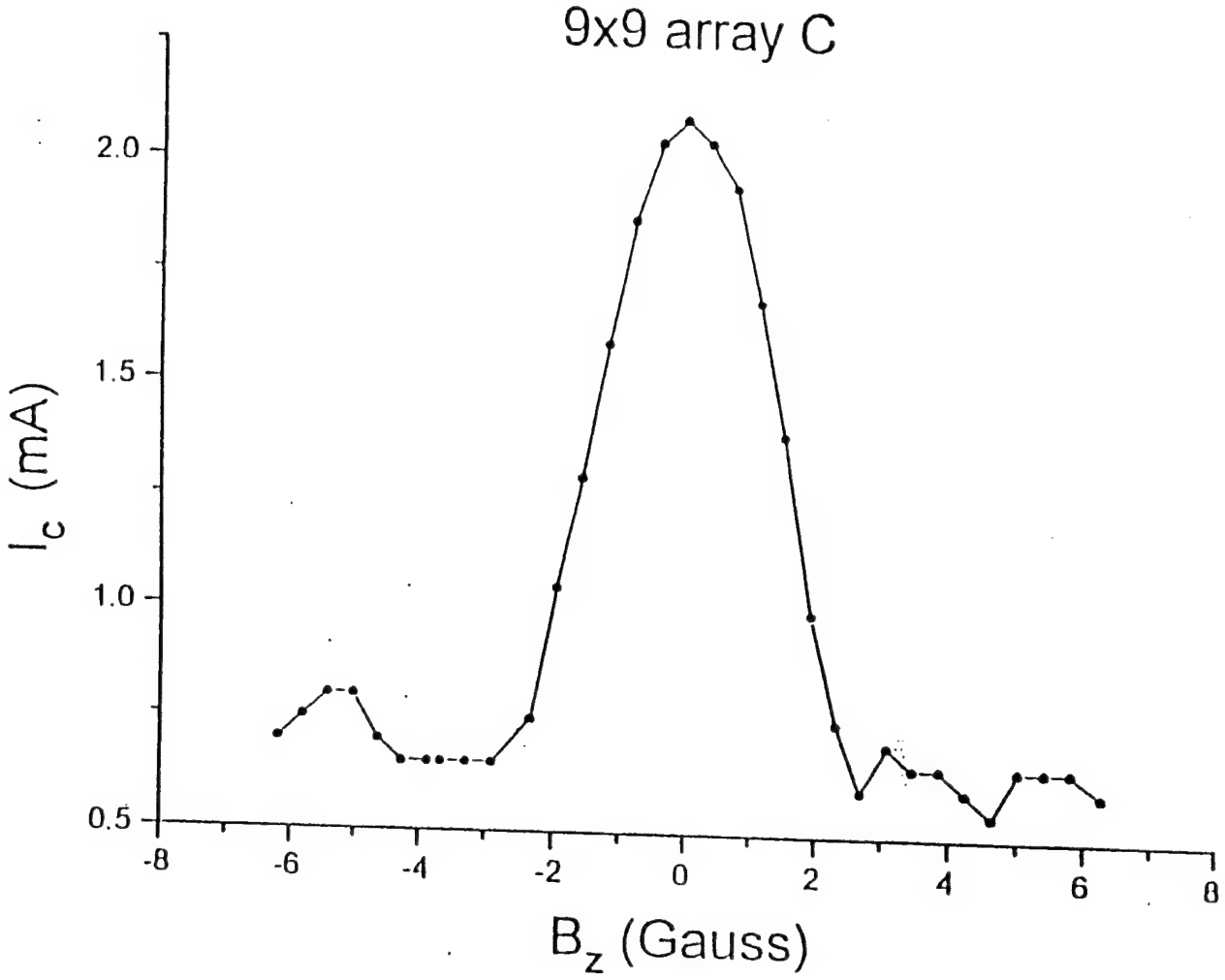

Figure 4. Critical current I_c, as defined by the dV/dI peak method, as a function of z-axis magnetic field for sample C. T = 77.5 Kelvin.

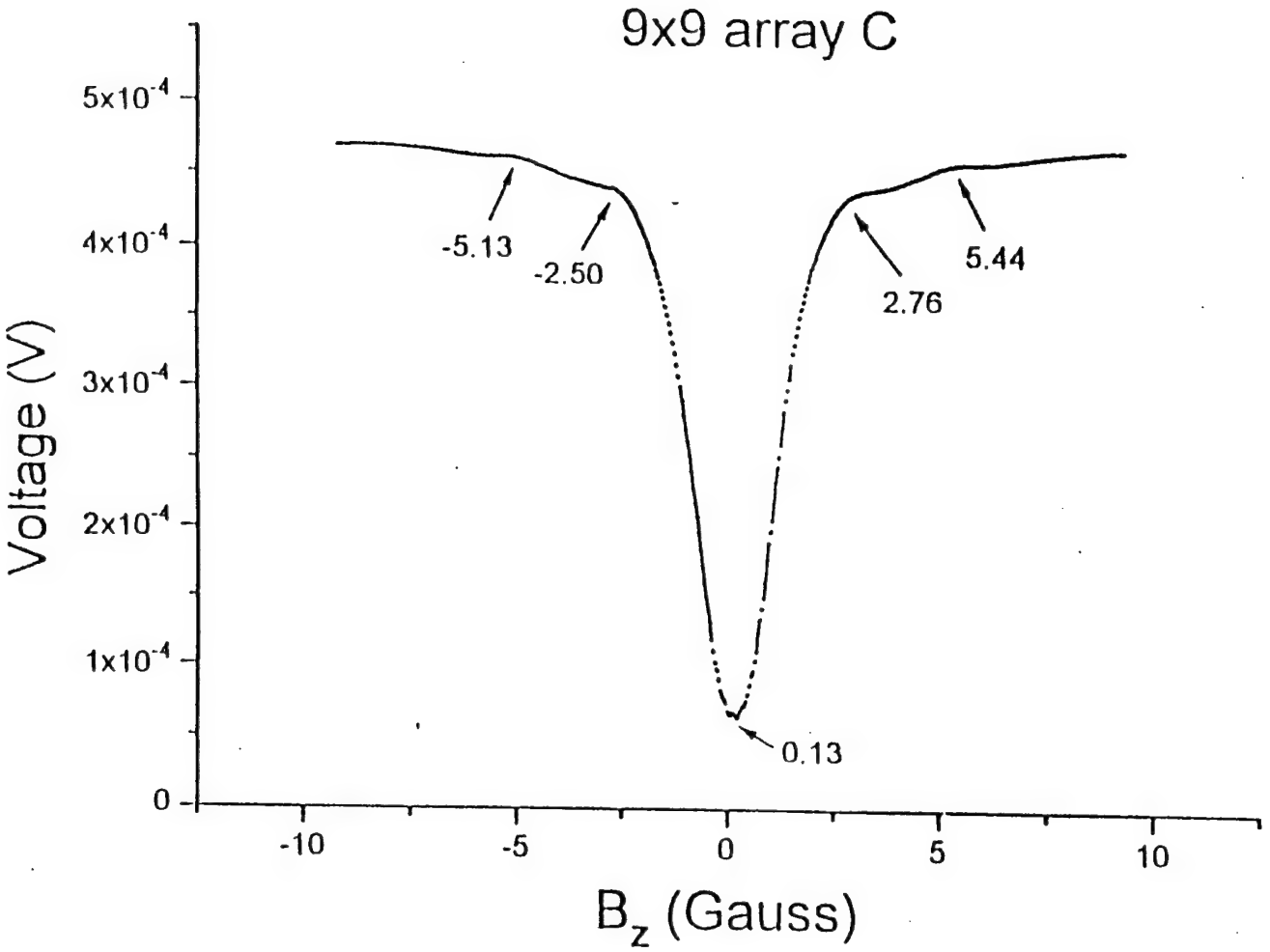

Figure 5 Voltage response of array C as a function of z-axis magnetic field. Bias current equals 1.9 mA. Arrows indicate central minima and the first two subsidiary maxima. T = 77.5 Kelvin.

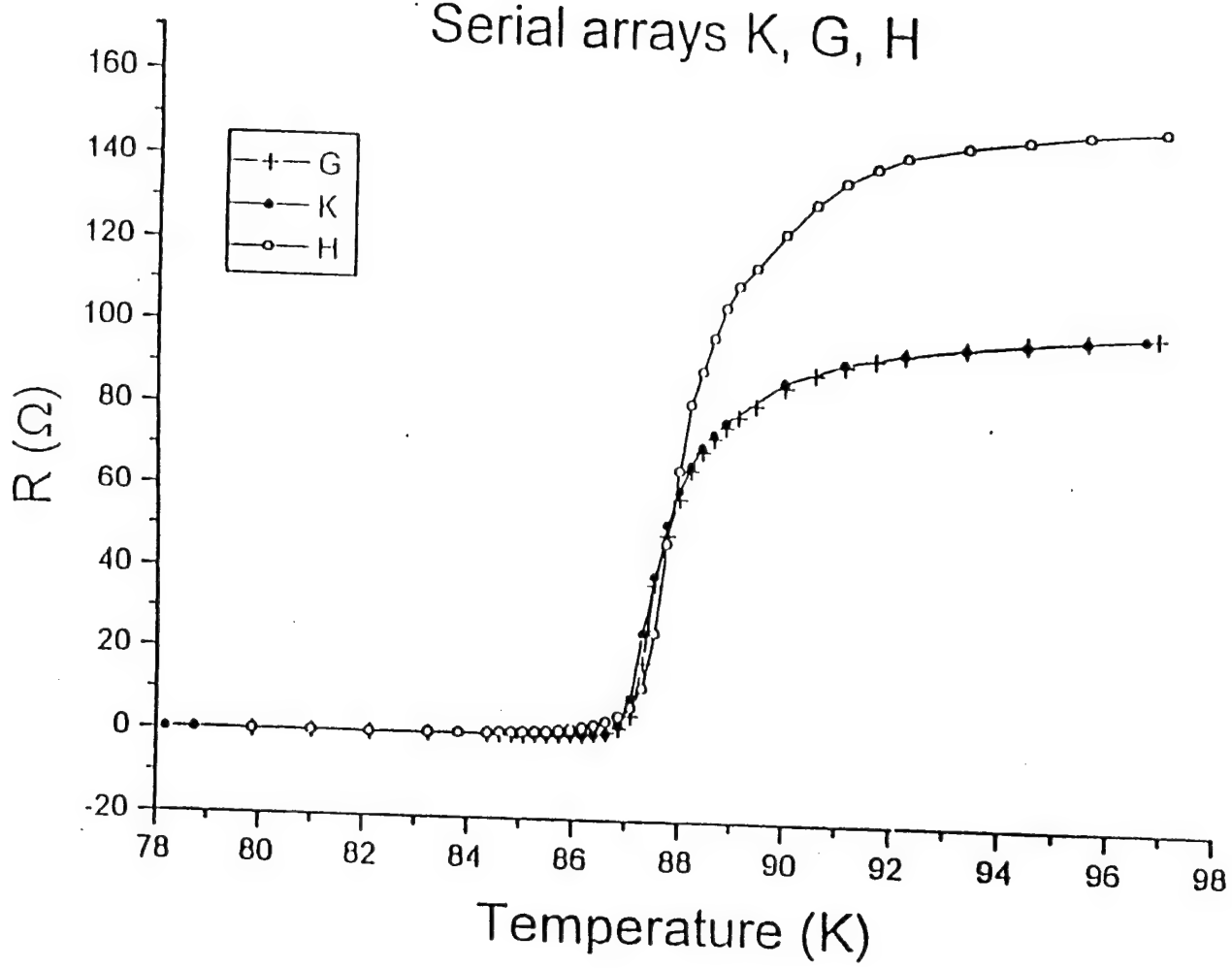

Figure 6 Resistive transition in zero magnetic field for 10 junction serial arrays K and G (3 μm wide junctions) and H (1.5 μm wide junctions).

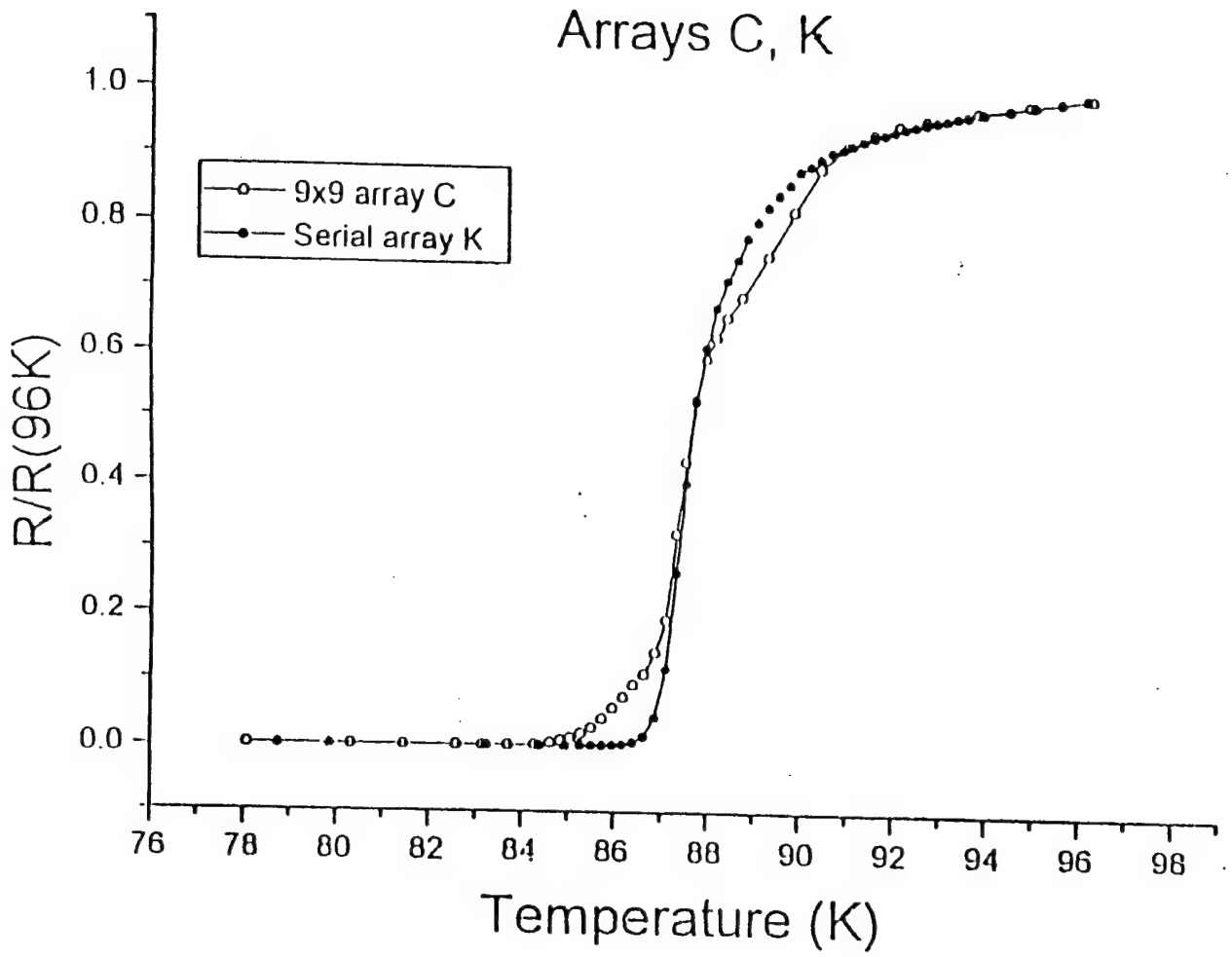

Figure 7 Resistive transitions of arrays C and K in zero magnetic field scaled to the resistance at 96 Kelvin for better comparison of features.

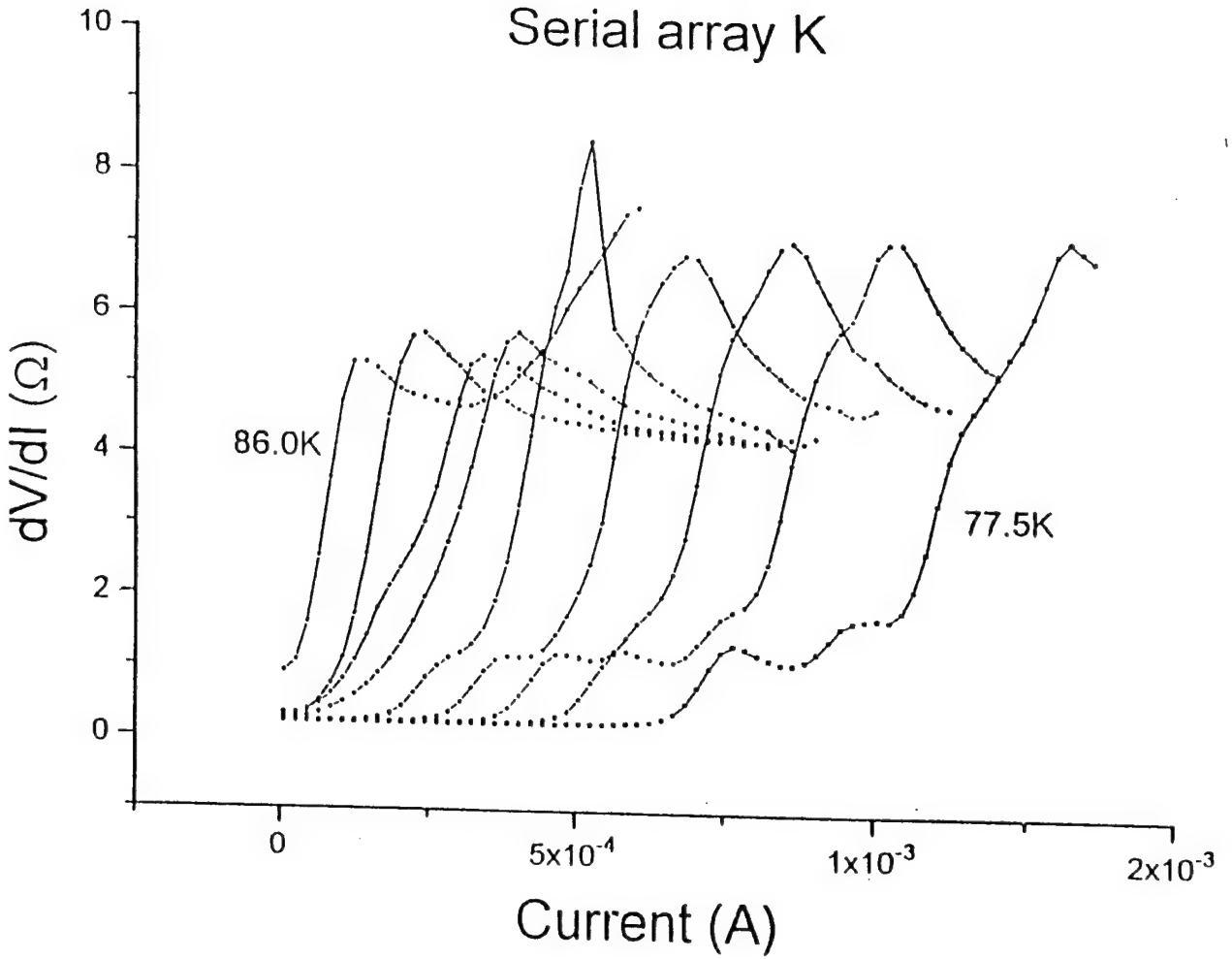

Figure 8 Plot of dV/dI taken from the curves shown in figure 9 Temperatures shown are 77.5, 78.1, 79.2, 80.3, 81.5, 82.6, 83.7, 84.8 and 86.0 Kelvin.

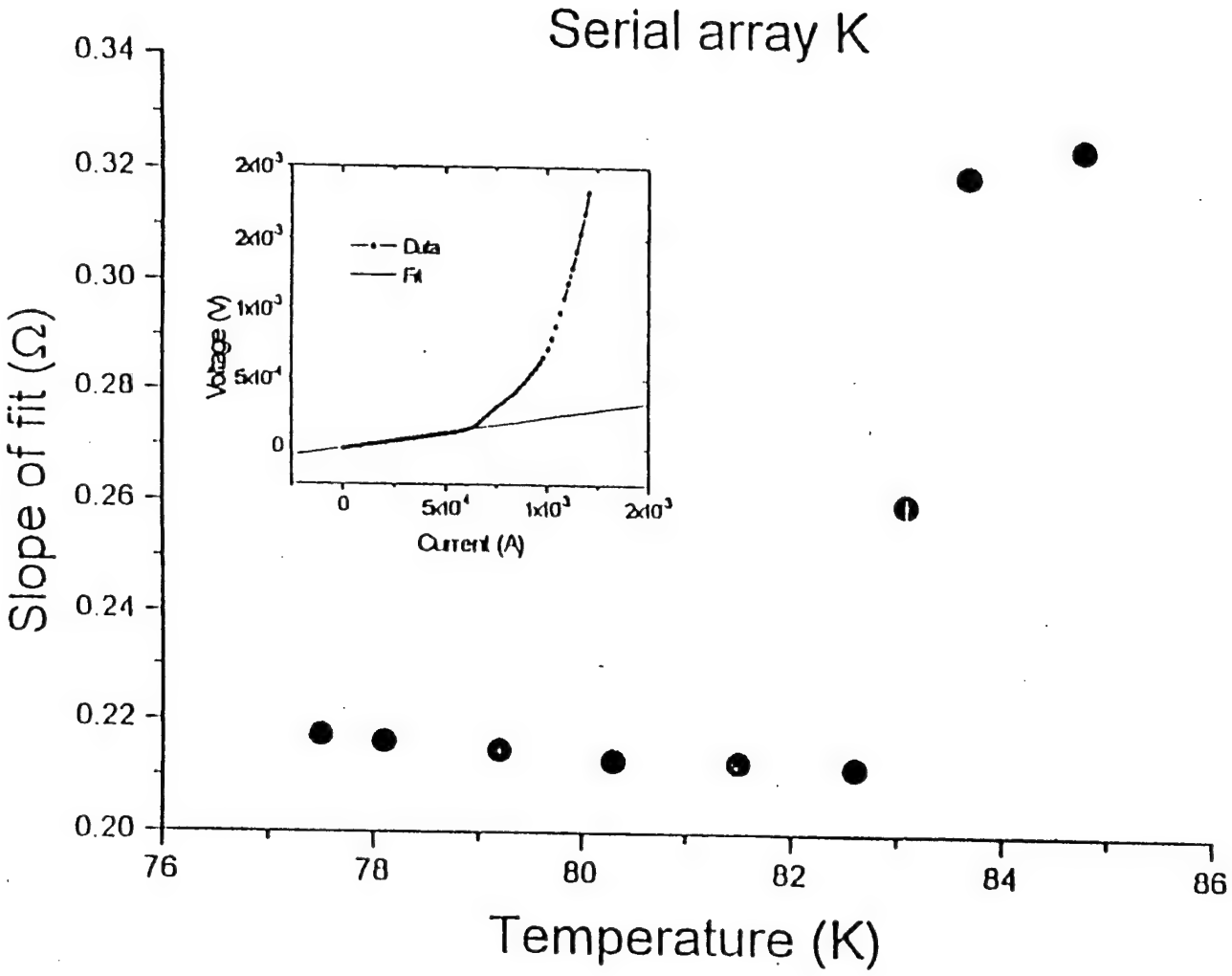

Figure 9 Resistance of 10 junction serial array K below superconducting transition, determined from slope of linear fit to IV curves. Inset shows IV at 78.1 K and linear fit.

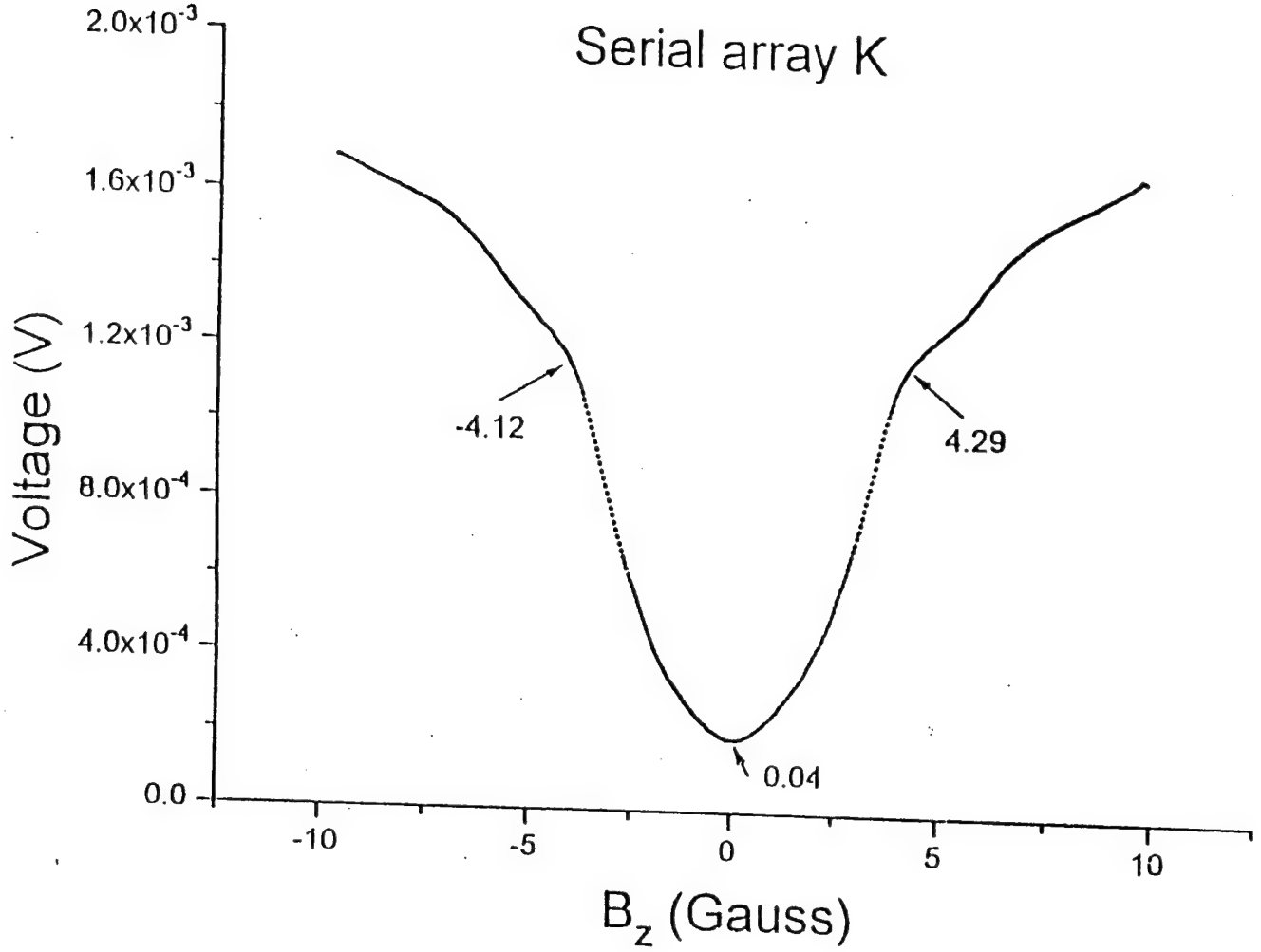

Figure 10 Voltage response of serial array K as a function of z-axis magnetic field. Bias current equals 0.72 mA. Arrows indicate central minima and the first subsidiary maxima. T = 77.5 Kelvin.

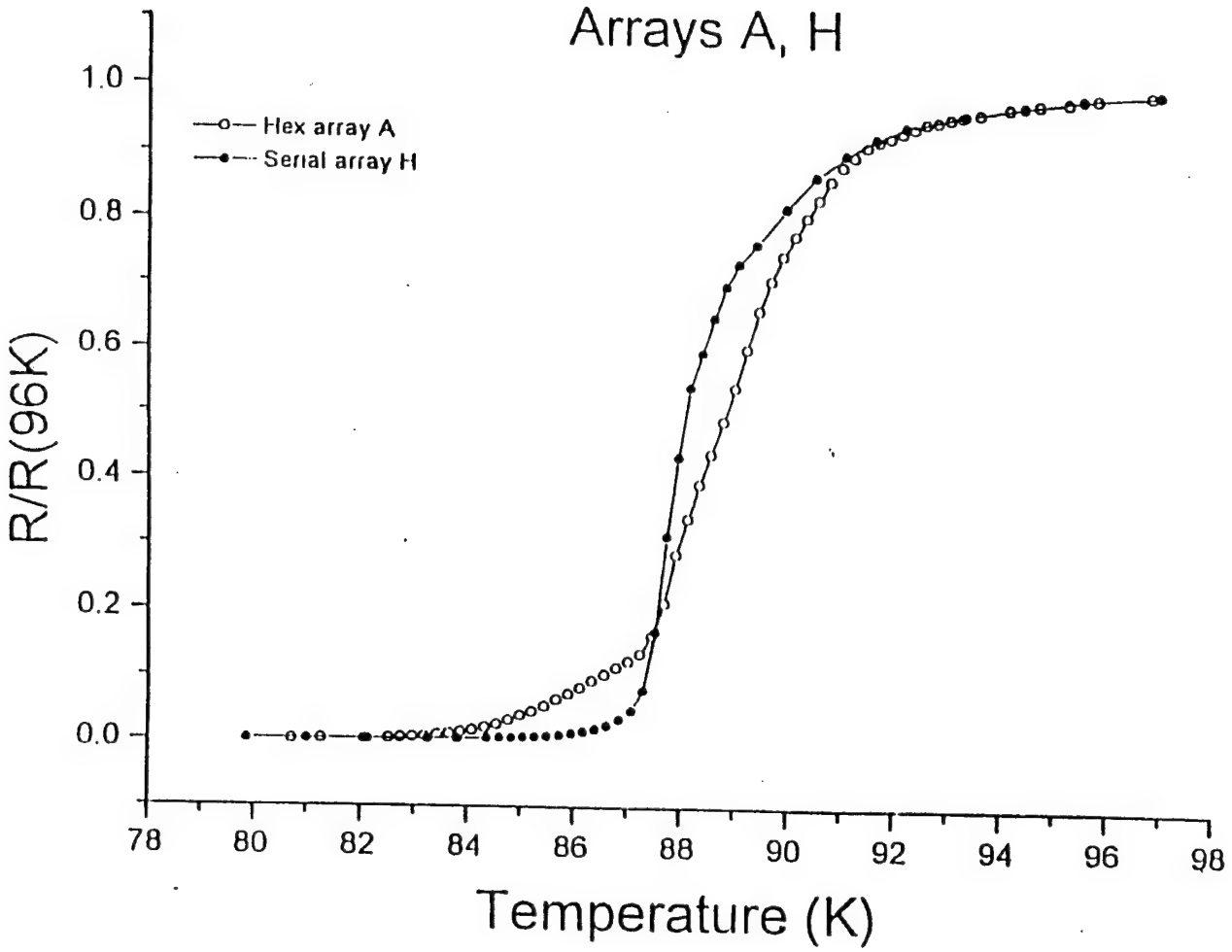

Figure 11 Resistive transitions of hexagonal array A and 10 junction serial array H in zero magnetic field. The curves have been scaled to the resistance at 96 Kelvin for better comparison of features.

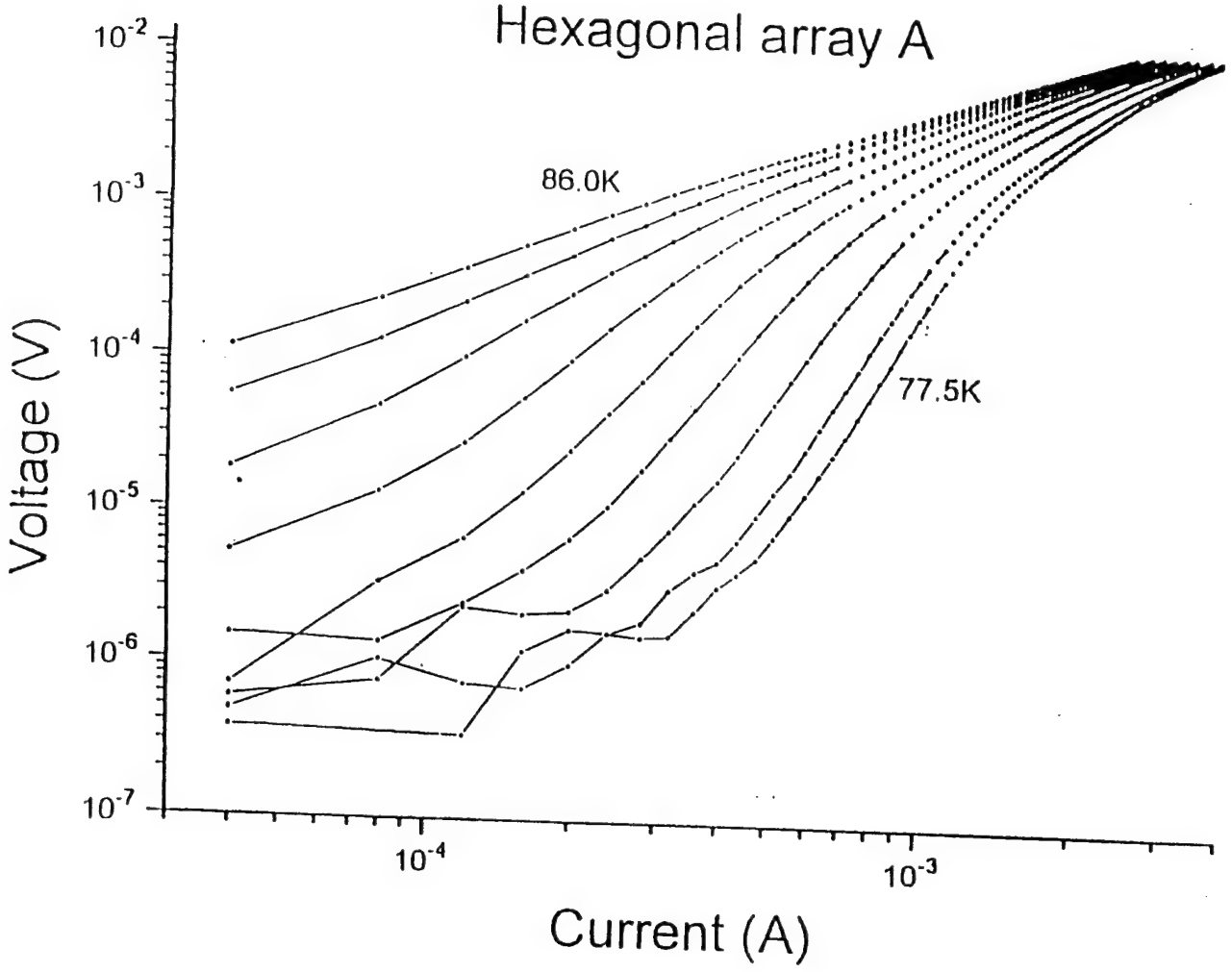

Figure 12 , Log-log plot of IV curves for hexagonal array A. Temperatures shown are 77.5, 78.1, 79.2, 80.3, 81.5, 82.6 83.7, 84.8 and 86.0 Kelvin.

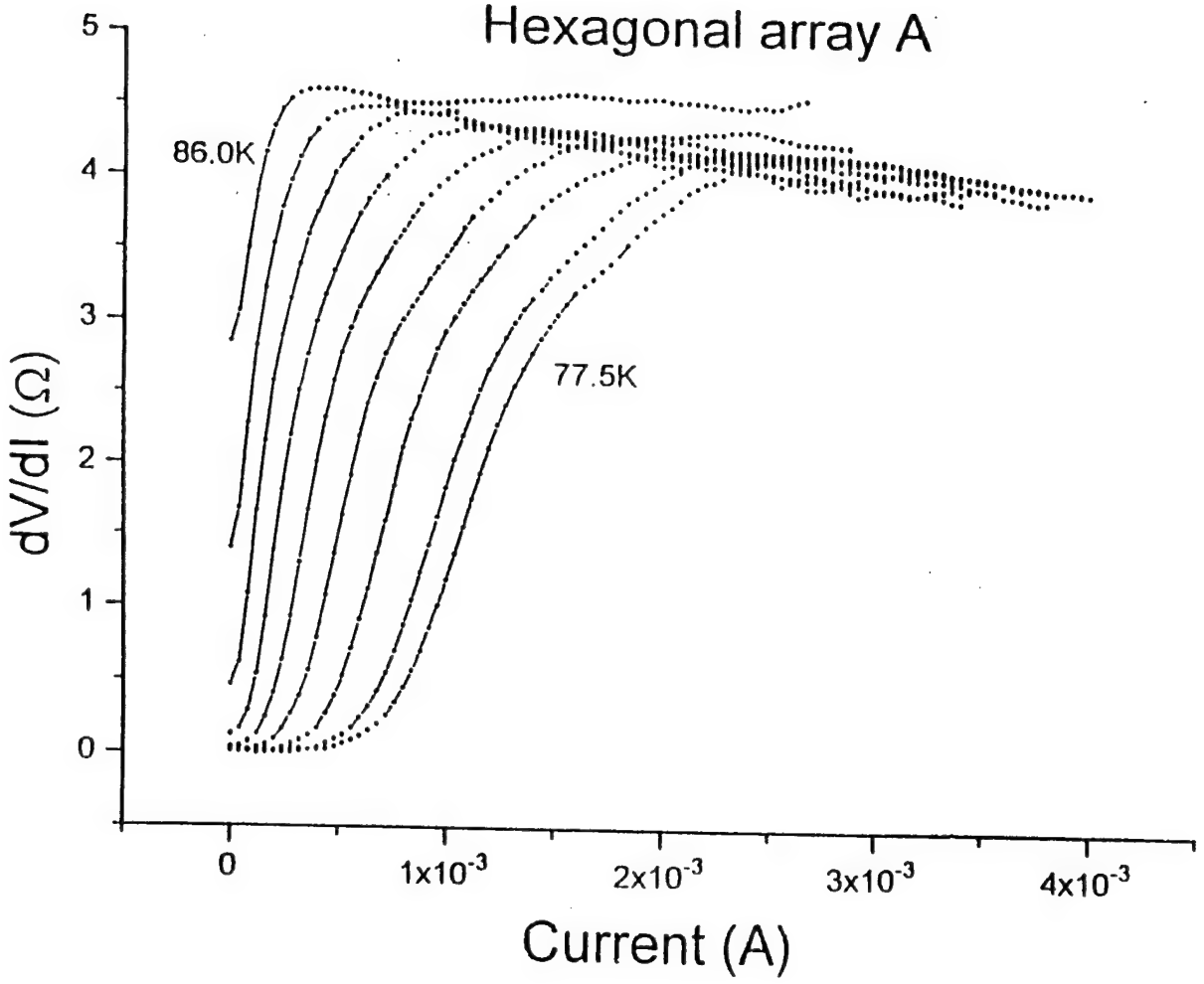

Figure 13 Plot of dV/dI taken from the curves shown in figure 12 between 77.5 and 86.0 Kelvin. Note the long resistive transition and subdued peaks compared to square lattice array C

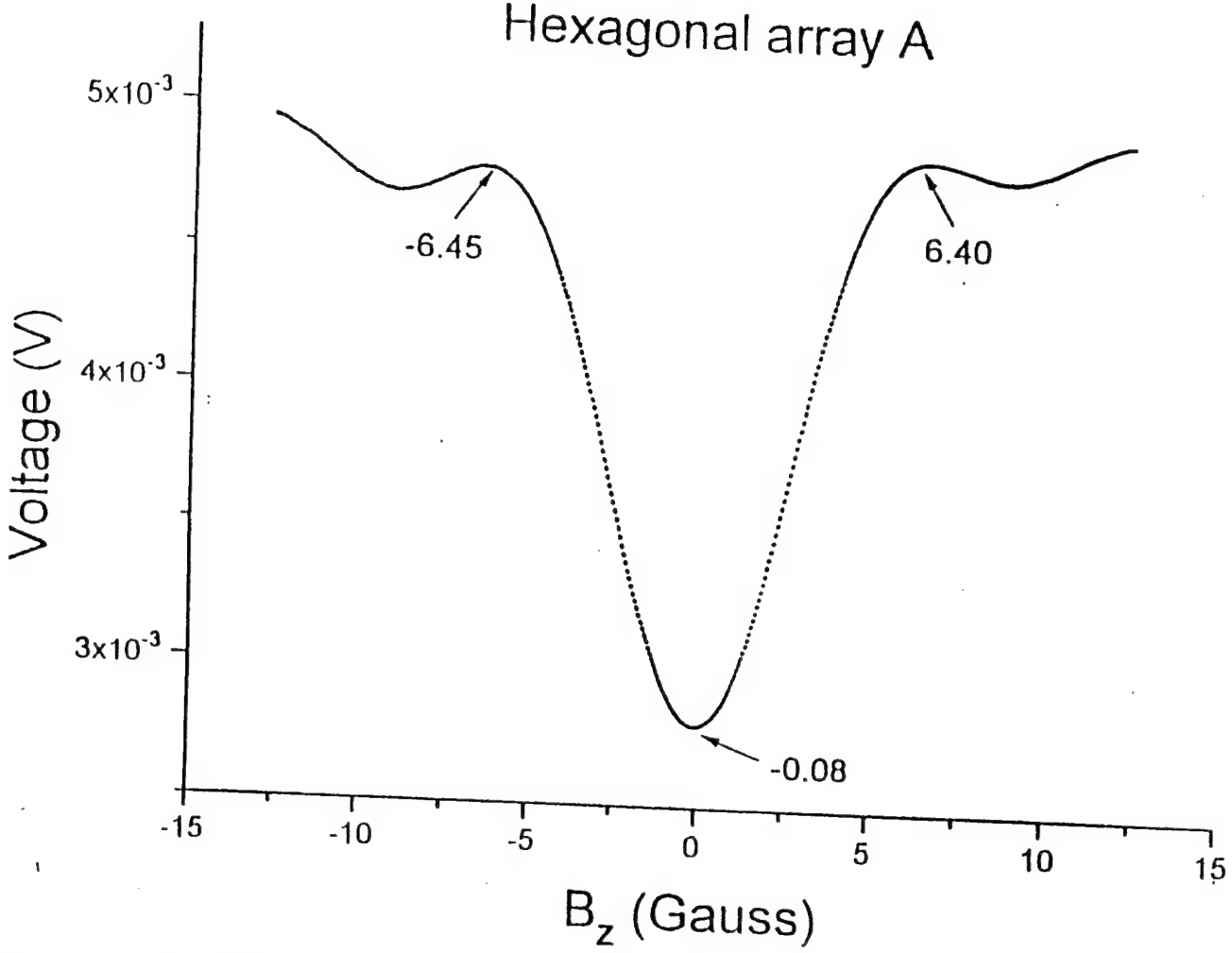

Figure 14 Voltage response of hexagonal array A as a function of applied z-axis magnetic field. Bias current equals 1.9 mA. Arrows indicate central minima and first maxima. T = 77.5 Kelvin.

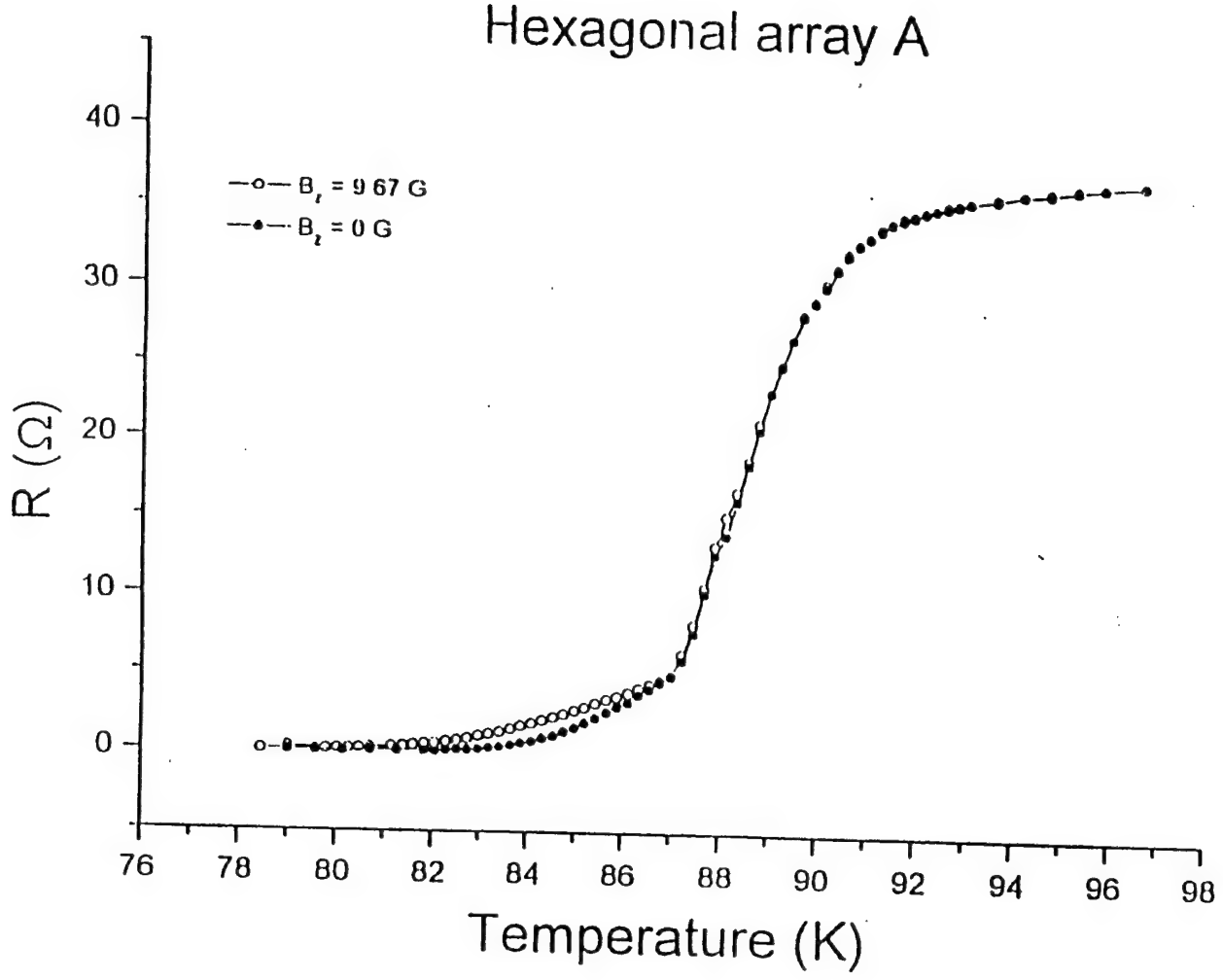

Figure 15 Field cooled resistive transition of hexagonal array A for two values of z-axis magnetic field. The sensing current equals 1 μA.

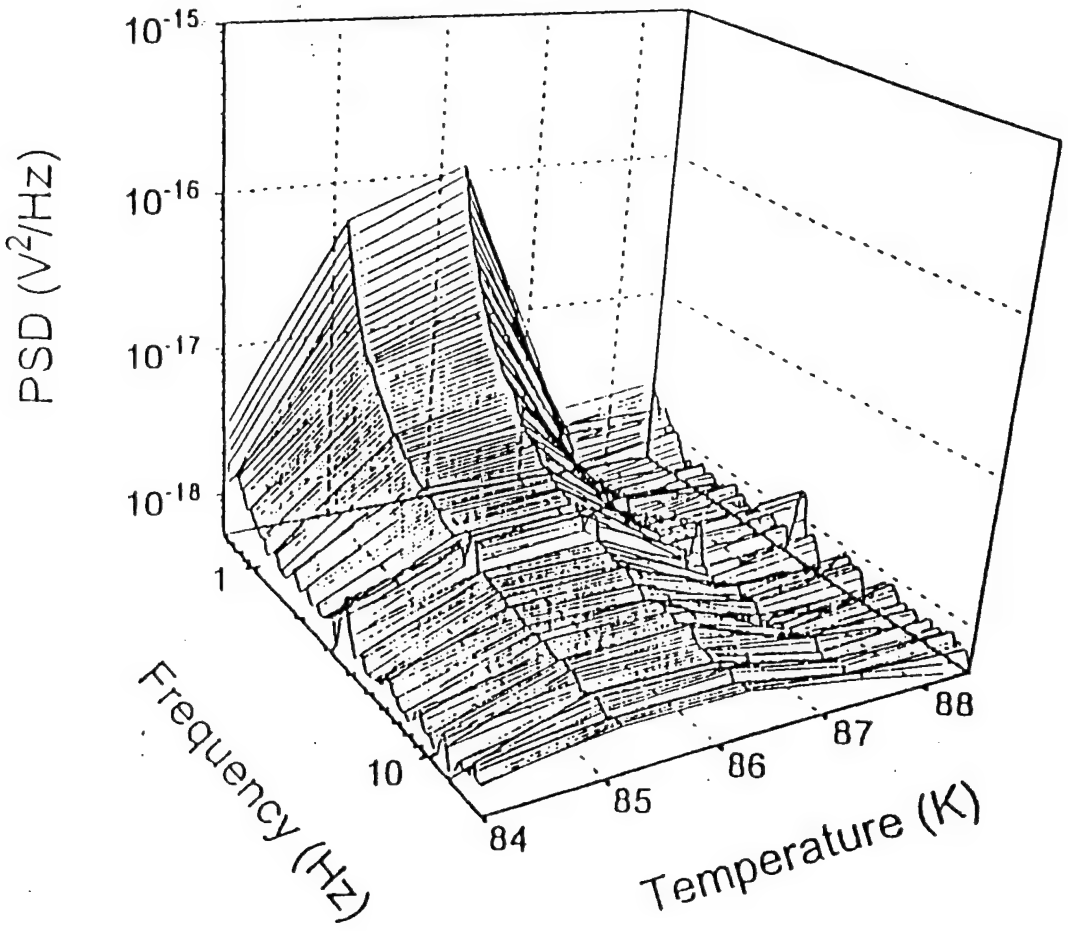

Figure 16 3D plot of the power spectral density (PSD) of the noise voltage across 9x9 array C as a function of frequency and temperature. PSD curves between 0.625 and 20.0 Hz are shown at 84.0, 85.1, 86.2, 87.3 and 88.4 Kelvin. The noise floor has not been subtracted. Grid lines connecting points at these temperatures are guides to the eye.

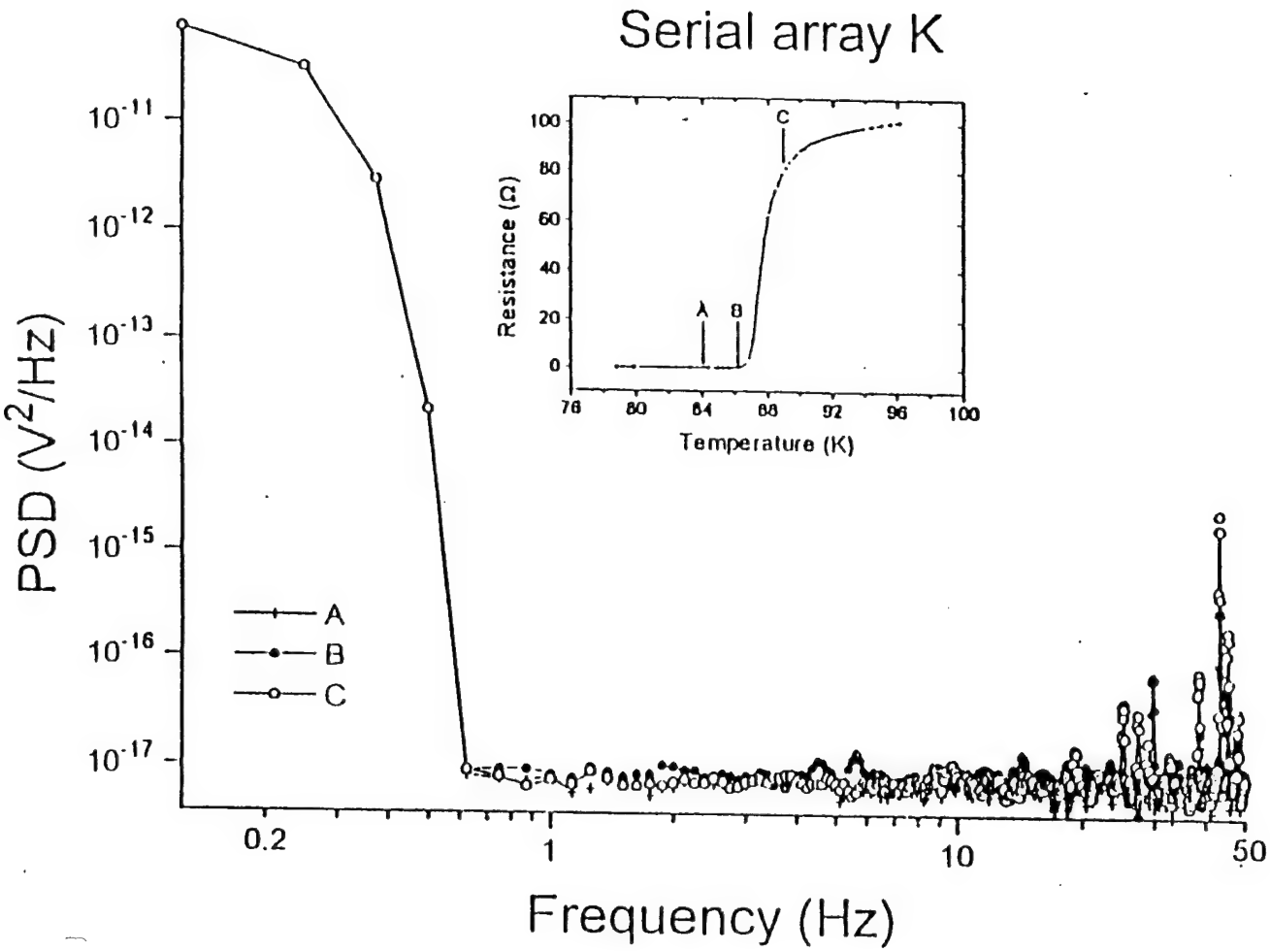

Figure 17 Plot of PSD versus frequency for 10 junction array K at 84.0, 86.2 and 88.4 Kelvin. The noise floor has not been subtracted. Inset shows resistive transition of array K.

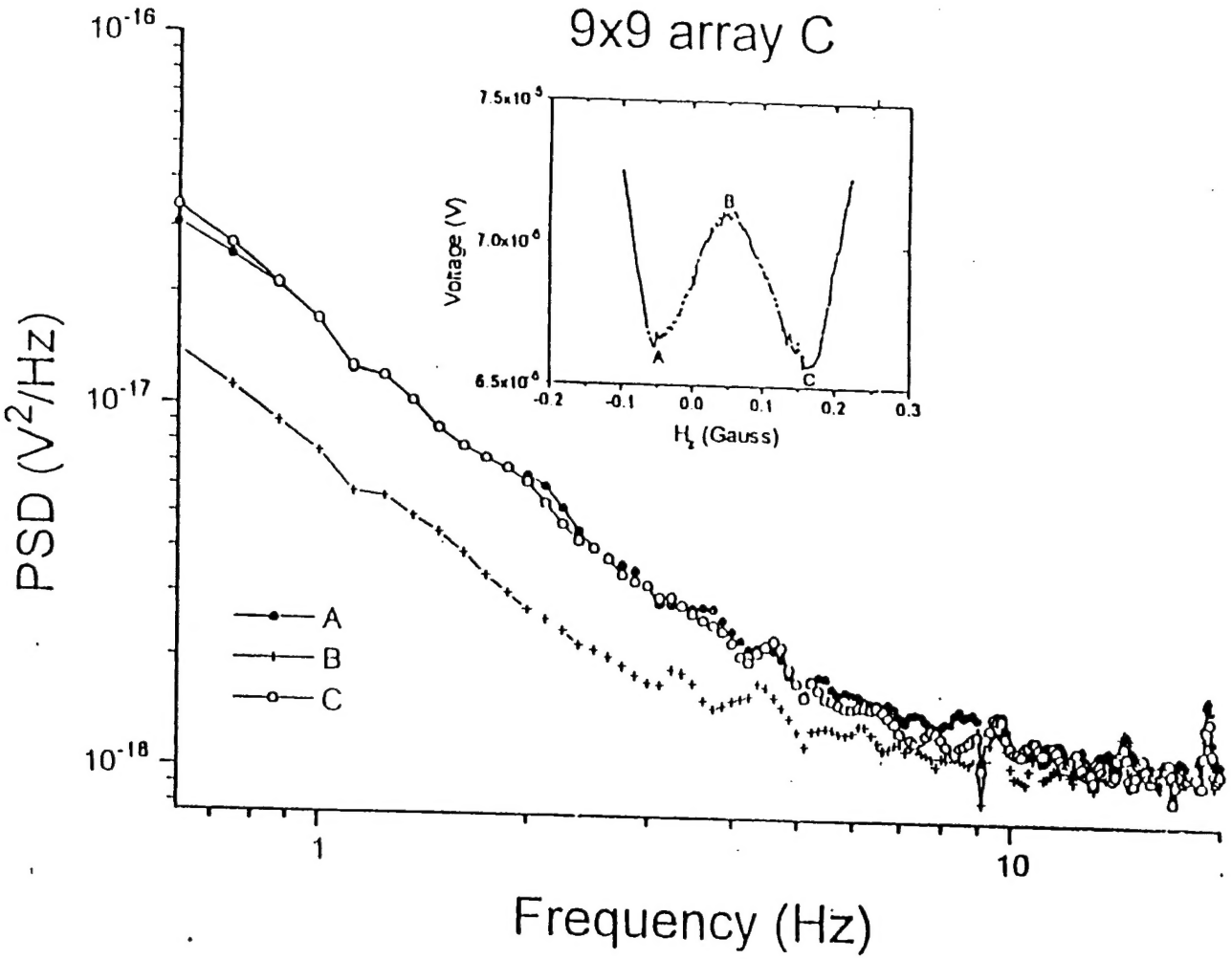

Figure 18 Plot of PSD versus frequency for 9x9 array C at magnetic field values corresponding to f = 0 (A), ½ (B) and 1 (C). The noise floor has not been subtracted. Inset shows magneto-response of array C. T = 77.5 Kelvin.

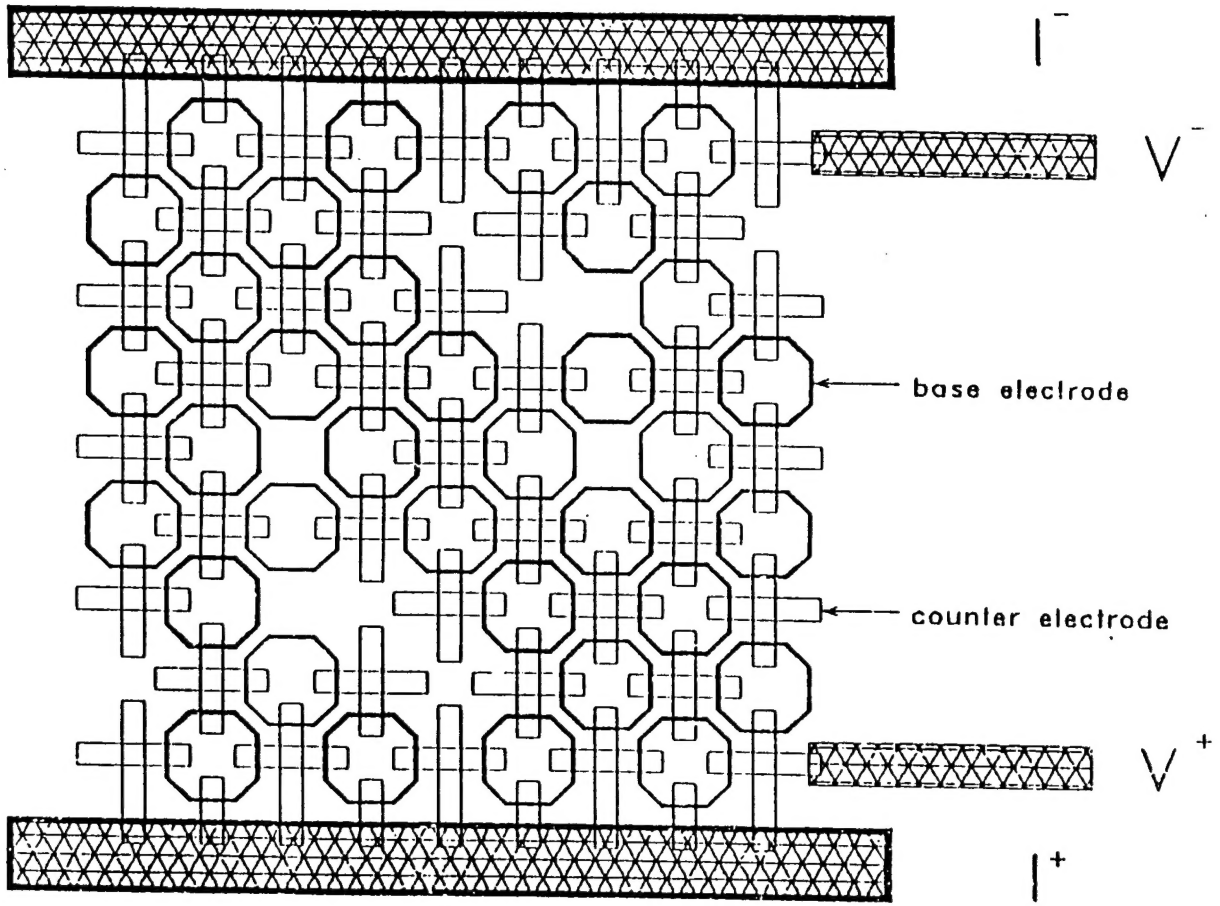

Figure 19 Schematic view of site-disordered 9x9 array B showing base electrode and counter electrode vacancies.

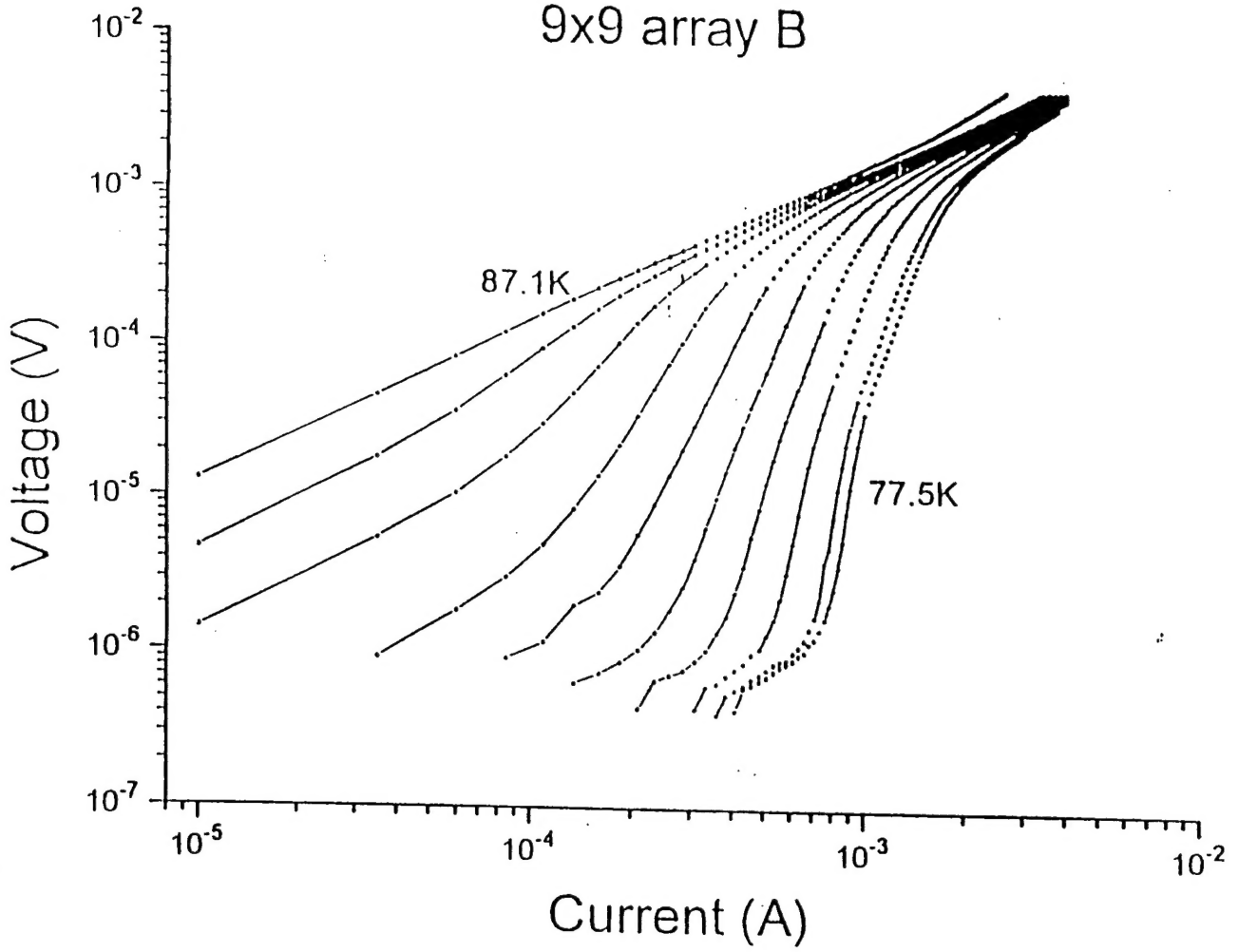

Figure 20. Log-log plot of IV curves for site-disordered 9x9 array B in zero magnetic field. Temperatures shown are 77.5, 78 1, 79.2, 80.3, 81.5, 82.6, 83.7, 84.8, 86.0 and 87.1 Kelvin.

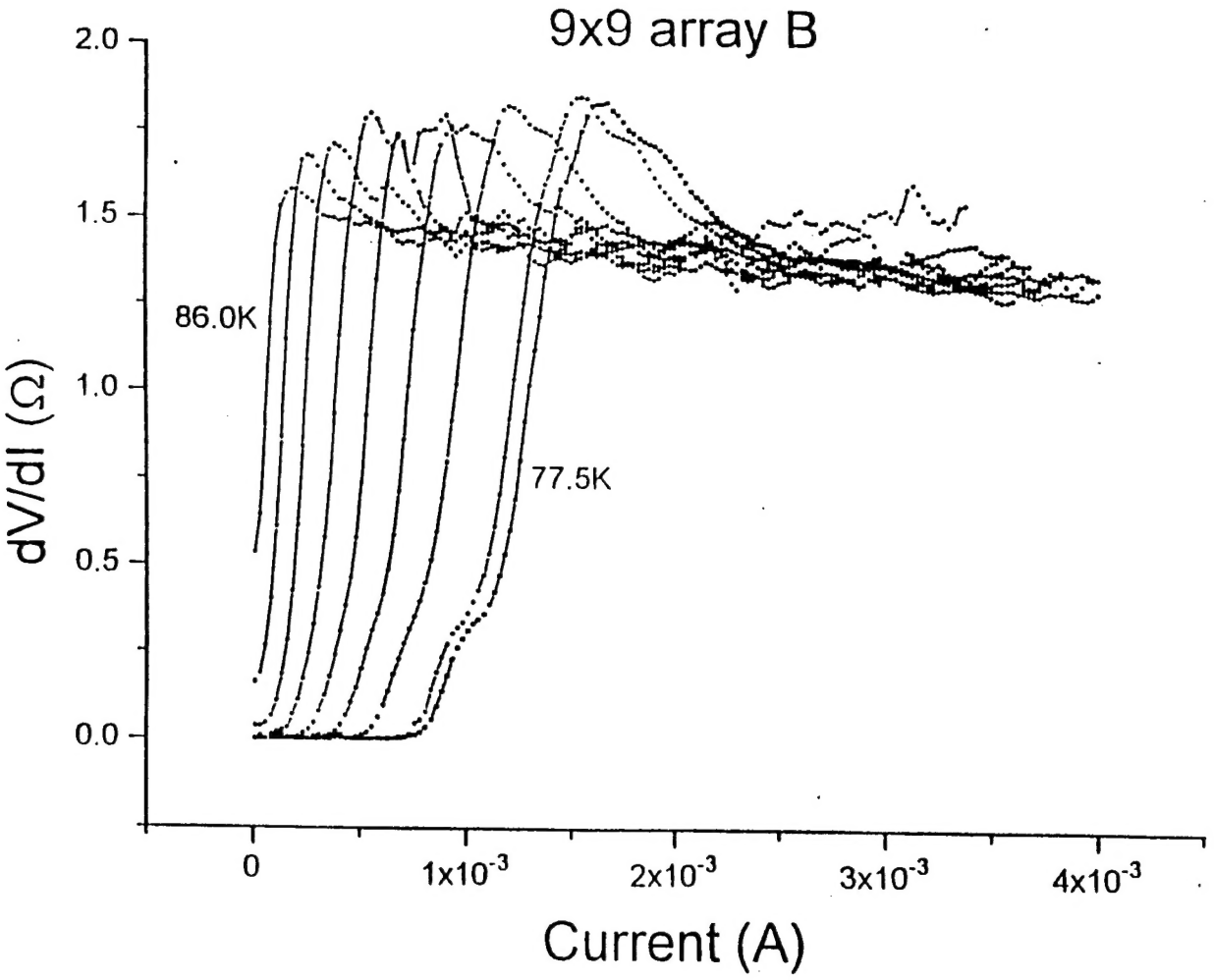

Figure 21 Plot of dV/dI taken from the curves shown in figure 20 . Temperatures shown are 77.6, 78.1, 79.2, 80.3, 81.5, 82.6, 83.7, 84.8 and 86.0 Kelvin.